# Computed Electronic Countermeasures System Implementation Investigation

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August 2000

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102-00622/

DREO CR 2000-066

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# Executive Summary

This report presents and discusses the issues involved in implementing *computed electronic countermeasures* (CECM) within a jammer system. Further, the report gives examples of an initial proof of concept demonstration system, with proposed upgrade path and estimated performance.

CECM is an important evolution in the capability and quality of countermeasures. CECM are countermeasures where the transmitted signal is digitally formed entirely or in large part using one or more programmable digital computers. Digital manipulation of a signal avoids many analog shortcomings, and allows independent and precise control of range, Doppler and amplitude for hundreds of closely spaced targets. CECM is flexible and programmable, is compatible with use of commercial-off-the-shelf (COTS) products and inherits the portability that comes with a software solution.

Surprisingly, the primary challenge in the implementation of a CECM-capable jammer is not computational power but data transfer bandwidth between the internal components of the system. A second challenge is availability of suitable high speed digital-to-analog converters subsystems in COTS form, although this is more a function of weak industry demand rather than technical feasibility. Although it was originally thought that analog-to-digital conversion speed and computation speed would be major hurdles, this report illustrates that recent improvements in these technologies make these aspects of CECM system implementation relatively straightforward.

A proof of concept demonstration system for CECM could be built largely from low-cost COTS components in two stages:

1. An initial wideband intercept system based on an Intel Pentium PC combined with a ADC and other COTS components. It could also have limited analog output capability.

2. An expanded version of #1 enhanced with a custom timing and control unit and a full analog output capability for wideband applications.

The initial demonstration system is sufficient to demonstrate capture of very wide bandwidth radar pulses in real time, and processing of these pulses in both real-time and slower-than-real-time. The initial system could also provide limited analog output capability for use in narrowband applications and to obscure limited patches of terrain in an image. The limited output capabilities could be sufficient to demonstrate live CECM against some airborne SARs, such as the C/X-SAR carried on the CV-580 aircraft.

The expanded system could be sufficient to demonstrate live CECM against high resolution radar systems such as ERS, RADARSAT, and the CV-580 airborne SAR. We estimate that from tens to hundreds of range targets (each with hundreds of azimuth components) are possible against most of these systems depending on the particulars of the radar and the detailed design and construction of the CECM hardware and software.

It is recommended that a full requirements specifications be made and a deeper analysis of system feasibility be performed. This report makes many assumptions of system performance from general sources of information which need to be confirmed or retired.

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# 1 Introduction

This report discusses the issues involved in implementing *computed electronic countermeasures* (CECM) within a jammer system. Further, the report recommends an initial proof of concept demonstration system, describes its predicted performance and outlines possible upgrade paths.

Computed electronic countermeasures are countermeasures where the transmitted signal is digitally formed entirely or in large part using one or more programmable digital computers. By using a digital representation of a radar pulse, the signal can be mathematically modified by computation in software to model the echo signals for arbitrary false targets.

CECM is an important evolution in the capability and quality of countermeasures. Digital manipulation of a signal is free of many analog limitations. For example, CECM achieves higher fidelity by eliminating intermodulation products. CECM allows independent and precise control of range, Doppler and amplitude for hundreds of closely spaced targets. CECM targets can be closely spaced in range even for pulse-compressed radars using long coded pulses. Most importantly, CECM is flexible and programmable, is compatible with use of commercial-off-the-shelf (COTS) products and inherits the portability that comes with a software solution.

Implementing CECM requires obtaining the radar pulse in digital form as baseband complex quadrature data in a memory accessible for processing. The *time of arrival* (TOA) of the pulse and the *time to transmit* (TTT) the modified pulse must be known and controlled to within a few nanoseconds. The signal/data handling, conversions and processing required for the CECM calculations must take place in the time between the TOA and the TTT. The signal/data handling and processing must also be able to handle a sustained stream of pulses at the radar pulse repetition frequency.

A proof-of-concept system should provide useful demonstration results at low cost and limited risk. The system must meet all constraints for timing, bandwidth and signal handling with available hardware for a variety of interesting demonstration cases. The evolution of the system over time and the ease of implementation must be considered when choosing equipment for the demonstration system.

## 2 System Implementation Requirements and Issues

The system requirements for CECM must support four major functions:

1. Conversion of the received RF pulse into a digital signal
2. Processing of the digital signal using one or more programmable digital computers
3. Conversion of the processed digital signal into a transmitted RF pulse
4. Timing and control

The received RF pulse must be translated down in frequency and then converted to a digital signal using analog-to-digital converter (ADC) technology. For CECM processing, it is most convenient for the digital signals to be represented in complex digital baseband format, also known as *quadrature* or *I/Q* data. This is true for both the received pulse and the computed output.

Processing of the digital signals is done using one or more software-programmable digital computers. These may be specialized digital signal processors, multiprocessors, or general purpose computers with fast arithmetic. The fundamental nature of the processing is finite impulse response filtering with filter coefficients which change every pulse.

Conversion from the digital baseband quadrature result to an RF transmission requires interpolation, digital-to-analog conversion technology, analog up-conversion, amplification and radiation.

Timing includes dedicated hardware able to generate timing strobes with approximately 1 ns precision under programmable control to synchronize transmissions to the incoming pulses and the radar illumination interval. The control function also includes such functions as scheduling and selection of techniques, adaptation to radar parameters, status reporting and user interaction.

Figure1 shows an overview of a generic system implementation for CECM from signal reception to transmission of the countermeasure signal.

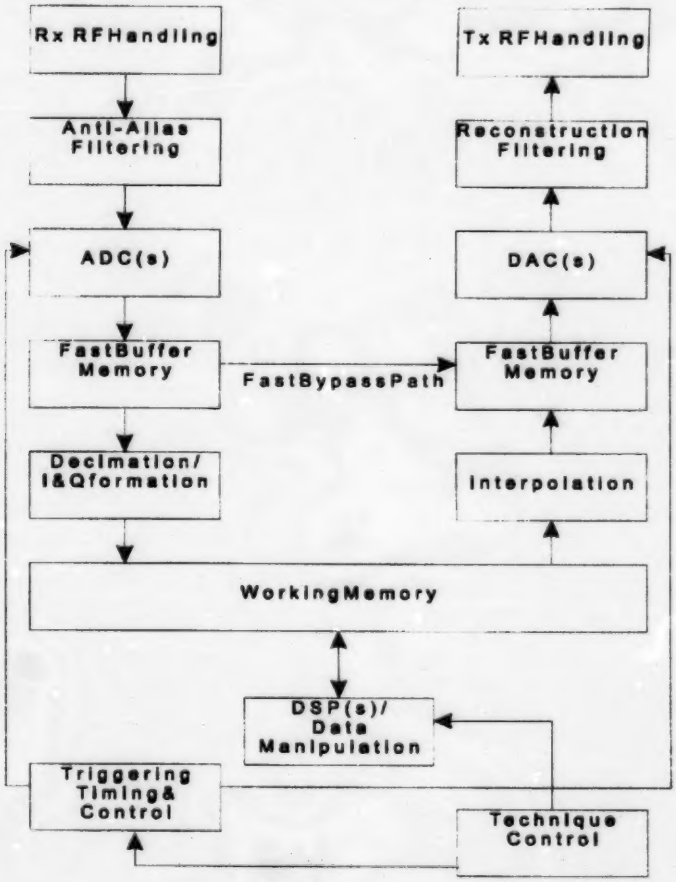


Figure 1: CECM Functional Block Diagram

The received signal must first be captured, frequency selected, amplified and mixed down to a lower IF or baseband frequency. This **receive RF handling** is common to most ECM systems and this is not dealt with in detail in this report.

The signal is next passed through an analog **anti-aliasing filter** and then digitized using one or more wideband **analog-to-digital converters (ADCs)**. If the analog electronics support quadrature mixing, there will be two ADCs. If the input analog signal is a bandpass signal mixed to a non-zero intermediate frequency, then a single ADC may be used, necessitating digital conversion to quadrature baseband at a later stage of processing.

The ADC or ADCs must operate at a sufficiently high sampling rate to ensure that the highest bandwidth signal anticipated is adequately sampled according to the Nyquist criterion. This sample rate could be on the order of 1 gigasample per second (GS/s) for high resolution radars. Such a high data rate necessitates the use of a **fast buffer memory** that can accept and store the incoming pulse data at the maximum required sample rate of the ADC.

Next, the signal will typically undergo **decimation** to reduce the data rate. If a single ADC was used, **digital quadrature formation** must be performed to get a complex baseband digital representation. These steps are important to reduce the amount of computation, and may have added benefits of suppressing noise and reducing memory requirements.

The complex baseband data is now available and may be transferred to a **working memory** where one or more **digital signal processing (DSP) computers** can access the data under software control. The computers may have general purpose or specialized DSP architectures, but will primarily be software programmable rather than using programmable logic or digital hardware exclusively.

The computed result corresponds to a modeled echo from a structured target or scene in complex digital baseband format. In a mirror image of the steps above, the data must be digitally **interpolated** to a higher data rate to increase the quality of the analog reconstruction. If a single digital-to-analog-converter (DAC) is to be used, the interpolation would include a **complex-to-real conversion**. Next, the data must be stored in another dedicated **fast buffer memory** so that the data can later be streamed out at a high data rate burst to the **digital-to-analog converter (DAC)**. Two DACs may be used if quadrature analog frequency up-conversion is used. An analog **reconstruction filter** is needed to recover the analog signal, followed by **transmit RF handling** to up-convert, amplify, and radiate the countermeasure signal.

The timing of DAC operation is precisely controlled by a **triggering, timing and control** unit which is essentially a precision counter which enables measurement of precise delays from the incoming pulse trigger to the DAC enable strobe. The time delay required is controlled by a **technique control unit** which also handles technique selection and scheduling, and other high level functions such as operator interface and status reporting.

### 2.1 Analog RF Reception, Mixing, Filtering and Transmission

Reception and transmission of RF signals is accomplished in the same way for computed ECM as for other active ECM approaches. Antennas are used to intercept and radiate the incoming and outgoing signals respectively. Filtering and amplifier stages are used for frequency selection, to increase the signal-to-noise ratio and to match power levels and impedances. Mixing translates the signals to lower frequencies to facilitate manipulation of the signal.

Two optional analog functions may further be required depending upon the system design:

1. Envelope/power detection of the pulse; and
2. Quadrature mixing to in-phase and quadrature components.

Detection may be done using a device such as a *successive detection log-video amplifier* (SDLVA). In combination with a voltage comparator, the SDLVA can be used to derive triggering information. Alternatively, detection may be done digitally using the data from the ADC's. Digital triggering is discussed briefly in section 2.5.

Quadrature mixing involves the use of two mixers driven by the same local oscillator, but with a 90° relative phase shift between the frequency references. These result in the in-phase and quadrature signal components, which allow representation of signals both above and below the reference frequency. The alternative is to use a single mixer and ensure only a single sideband passband is used either above or below the reference frequency.

Quadrature mixing produces a complex baseband signal in the analog domain, rather than digitizing a real bandpass signal and doing quadrature formation in the digital domain. Use of analog quadrature mixing dictates that two ADCs will be needed, however the added complexity is offset by the fact that a lower sampling rate can be used. Furthermore, avoiding digital quadrature formation simplifies other parts of the system and can preserve resources for generation of structured false targets. This is discussed in some detail in the following subsection.

### 2.2 Analog-to-Digital Conversion and Fast Buffering

Analog to digital conversion and buffering of the digitized signal are intended to convert the analog signal into a digital signal at a constant sampling rate high enough to preserve the pulse information, and provide asynchronous access to the stored data by digital computing hardware.

There are three key factors to consider with respect to the analog to digital conversion:

1. Whether one ADC or two ADCs will be used per antenna channel[1]
2. Maximum sampling rate and sampling rate selection
3. Precision of the ADC(s)

[1] For some applications it may be desirable to have separate antenna channels for direction finding, interferometry, or polarimetry. Here we will consider the requirements for a single channel, which apply equally to additional channels.

There are two additional key factors to consider related to the fast buffer memory:

4. Ability to accept data at the maximum sampling rate of the ADC(s)
5. Capacity of the buffer memory

Factor 1 above is essentially a choice between 1) digitization of a single bandpass signal centered at a non-zero intermediate frequency (IF) using one ADC; and 2) digitization of a pair of baseband quadrature signals centered at zero frequency using two ADCs.

So-called *bandpass* or *real* sampling is beneficial because it requires only one ADC per antenna channel, however it typically requires 3 to 4 times higher sampling frequency than the quadrature sampling approach. Other commonly cited benefits of bandpass sampling are precision of the phase measurements, however this is not a significant factor in the CECM application where phase errors on the order of 10 degrees can be tolerated [1]. A major drawback of bandpass sampling is the need to perform quadrature formation in the digital domain at relatively high speeds, which imposes additional complexity and constraints on the digital part of the system. This is discussed in more detail in section 2.3.

The *quadrature sampling approach* has the benefit of allowing lower sampling rates (and smaller overall data volumes) for a given signal bandwidth, or equivalently, allowing higher bandwidths for a given maximum sampling rate of the ADC. Another major benefit (discussed in the next subsection) is that it eliminates the need to form the quadrature baseband signal digitally, simplifying the digital portion of the system. An obvious drawback of quadrature sampling is the need to purchase, power, synchronize and house two ADCs.

The maximum sampling rate for the CECM system should be as high as possible, since the highest resolution new radars are always pushing the limits of ADC technology and the laboratory CECM system may have to keep up with this pace. As we have stated, the quadrature sampling strategy maximizes the bandwidth of the CECM system for a given sampling rate. For a quadrature sampling approach the maximum required sampling rate will be about 120% of the maximum radar bandwidth, whereas the maximum required sampling frequency for bandpass sampling system would be about 300% to 400% of the maximum radar bandwidth [2].

The sampling rate should be adjustable to reduce the overall data volume, data transfer and computation in applications where the threat has bandwidth smaller than the maximum system bandwidth. This reduces or eliminates the need for digital decimation, which is discussed in section 2.3. A low sampling rate can also save memory, though this is rarely a major constraint.

A point to remember is that the effective noise will increase if the sampling rate is reduced without narrowing the analog bandwidth of the anti-aliasing filter preceding the ADC(s).

The precision of the ADC can be considered to have two main aspects:

- The precision and dynamic range of amplitude encoding
- The time accuracy of the sampling points

One common figure of merit used to partially characterize both[2] of these aspects is the *effective number of bits* (or *ENOB*), quoted for a specific operating frequency and test signal frequency[3]. This approach equates the total noise power after digitization of a pure sinusoid to that predicted for an ideal ADC with a specified number of bits (the ENOB value itself). ENOB is a good measure of ADC performance provided that the test signal frequency is close to the highest expected signal frequency, and the ADC noise power is relatively evenly distributed over the spectrum. The *spurious free dynamic range* or a spectrum plot should be consulted to verify that the manufacturer's specifications preclude large spectral spikes or harmonics that are much higher than the noise floor.

The precision in ENOB required for a given mission depends upon the dynamic range required and the minimum acceptable signal-to-noise ratio at the input of the CECM system. The basic idea is to ensure that the needed SNR over ADC quantization noise is provided even when the signal is minimum (i.e. lowest power threat at maximum range), while preventing saturation of the ADC when the signal is at its maximum (i.e. highest power threat at the minimum expected range). The use of an *automatic gain control* or *AGC* would extend the dynamic range without additional ADC precision, but this could be limited in a dense environment where CECM may have to jam multiple radars at the same time.

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2 At first consideration the ENOB would seem to deal only with ADC precision. Timing jitter, however, normally appears as a higher noise floor. Therefore the ENOB specification includes the effects of timing jitter by equating it with quantization noise for an equivalent ideal converter with fewer bits.

3 It should be noted that ENOB typically goes down as operating frequency and test signal frequency go up. This is another argument in favour of quadrature sampling over bandpass sampling.

The total required dynamic range $W_{total}$ can be expressed in dB as the sum of the dynamic range variations due to different effective radiated power (ERP) and due to different ranges, plus the minimum acceptable signal-to-quantization-noise ratio.

$$W_{total} = W_{ERP} + W_{range} + SQNR_{min} \quad (1)$$

$W_{ERP}$ is the decibel difference in threat radar ERP, while $W_{range}$ is the power variation due to difference in $R^2$ falloff at the maximum and minimum threat ranges. $W_{range}$ is simply the squared ratio of the maximum to minimum range expressed in decibels. $W_{range}$ changes by 6 dB per doubling of distance between minimum and maximum range.

Given $W_{total}$, the required effective number of bits can then be estimated as:

$$ENOB = W_{total} / 6\ dB_{per\ bit} \quad (2)$$

Normally 6dB of SQNR is provided by each bit of ADC precision. For a 4 bit ADC (as used in RadarSat), the SQNR is 24dB. If we assume a 24 dB minimum SQNR, a two-fold variation in ERP, and a two-fold difference in maximum and minimum range, then 5.5 effective bits are sufficient. This example is fairly representative of the spaceborne SAR ECM case, which is not demanding from the point of view of dynamic range.

Common 8 bit ADCs which may achieve 6.5 ENOB would provide 15 dB of instantaneous dynamic range beyond the basic 4 bits of common digital RF memories (DRFMs), i.e. 39 dB total dynamic range. It may be possible to extend this by 3dB for every factor of two oversampling if filtering is used to reduce quantization noise. In combination with an AGC, such a scheme should be useful for many cases of interest.

The speed of the fast buffer memory must be matched to the maximum required sampling rate, which usually dictates that there will be limited physical distance between the ADC and its corresponding buffer memory. Normally the stream of data from the ADC will be stacked side-by-side into longer word lengths and then loaded into a wide memory which can operate at a clock rate several times slower than the ADC sample rate.

The capacity of the fast buffer memory should be large enough to handle the longest expected pulse at the corresponding sampling rate. This can be calculated with the following equation:

$$Memory_{per\ pulse} = F_s\, \tau\, M_s \quad (3)$$

Here, $F_s$ is the sampling rate, $\tau$ is the pulse width, and $M_s$ is the memory per sample in bytes. Note that $M_s$ could account for the memory required for a complex sample pair in the quadrature sampling case.

For a relatively high sample rate of 1 GS/s combined with a relatively long pulse width of 50 µs, and assuming 8 bits per sample for each of the in-phase and quadrature channels, 100 kilobytes is sufficient to store a long high bandwidth pulse. This is a fairly small amount of memory by current standards, therefore quantity of memory should not be a significant factor in CECM system design.

### 2.3 Digital Quadrature Demodulation and/or Decimation

*Digital quadrature demodulation* is necessary if the bandpass sampling approach (with one ADC) is adopted. As explained above, the sampling rate required for bandpass sampling is higher than that required for quadrature sampling. For this reason digital I/Q demodulation usually includes digital decimation processing which reduces the data rate to that equivalent to the quadrature sampling case. This reduces data volumes and downstream computational load.

If quadrature sampling is used, however, it may still be useful to perform decimation to reduce the data rate for the quadrature data stream while reducing noise. This can be done if the original signal is intentionally oversampled. Oversampling may be done in order to reduce the effective quantization noise (and increase apparent ENOB), or to meet the Nyquist criterion for a fixed analog anti-aliasing filter. The effective bandwidth can then be reduced during the low-pass filtering which usually accompanies decimation processing. Again, the result is higher SNR, smaller data volume, and less computation to process the same information.

For example, if a factor of 16 was used in oversampling then decimated by 16, the data size would be reduced to $1/16^{th}$ that sampled with the benefit of 12dB better SNR. However, this requires additional bandwidth, time for decimation and time for interpolation of the data after processing.

Both digital quadrature demodulation and ordinary decimation require computational resources to accomplish the necessary filtering and/or digital mixing operations. These operation could be accomplished using computer algorithms, or using dedicated hardware. If there are sufficient computing resources available then the former method could be used. Otherwise, dedicated hardware digital receiver integrated circuits are available to accomplish this specific task, but at the expense of additional hardware complexity and somewhat less flexibility.

Currently, neither the hardware nor software approach to digital quadrature demodulation is able to keep up with the maximum data rates from the ADC (or ADCs). Therefore it will typically take two to ten times longer to accomplish digital quadrature formation than it does to capture the data, depending upon the sampling rate selected.

### 2.4 Data Transfer, Working Memory and Signal Processing

Of data transfer, memory and signal processing, the major challenge for a CECM system is data transfer bandwidth between the fast buffer memories and the computer or computers which will perform the signal and data processing. For multiprocessor approaches, transfer of data between processors may also prove significant.

As we have seen in the previous section, memory on the order of a few hundreds of kilobytes is more than sufficient to store a typical radar pulse. Fast memory is available in multiple megabyte quantities at very reasonable costs, so it is apparent that there will be little difficulty in building systems with sufficient memory to store and manipulate hundreds of pulses at multiple stages of processing.

Sufficiently fast communication with memory, however, remains a significant issue. Typical low-cost high-speed bus technology is limited to on the order of 100 megabytes per second (MB/s). Since the ADC may operate at sampling rates as high as 1 GS/s or above, it is clear that transfer of the pulse out of the fast buffer memory may take several times longer than the time required to sample the pulse. If both the bandwidth and the duty cycle are very high, there will be limited time within the PRI for processing unless data transfer bandwidth is enhanced.

For very ambitious CECM schemes or challenging combinations of high bandwidth, high duty cycle and high PRF, multiple processors will be needed. The basic function of the CECM signal processing will be finite impulse response (FIR) filtering using either the time or frequency domains. The filter coefficients will be changed on every pulse, requiring a relatively high rate of transfer of coefficients into the processor memory.

The problem of fast implementation of FIR filters has been well studied, and will not be covered in detail here. It is sufficient to note that multiprocessor partitioning of both time domain convolution and the Fast Fourier Transform (FFT) algorithms has been studied widely and can be directly applied to the CECM application.

For simple cases, a single powerful general purpose processor is sufficient to provide useful CECM such as image patches or closely space range targets with independent arbitrary Doppler modulations. Some examples against various radar systems for a specific single processor demonstration system are given in section 3.4.

### 2.5 Digital-to-Analog Conversion, Buffering and Signal Interpolation

Digital-to-analog conversion, output buffering and signal interpolation stages are necessary to generate an analog signal representing the echo of the radar pulse from a structured false target or scene. This signal is then translated upwards to RF frequency, amplified, and radiated back to the threat radar.

The digital-to-analog converter (DAC) converts the digital data into an analog signal. Normally the DAC will work at a much higher rate than the Nyquist frequency. This allows looser specifications on the analog reconstruction filter which follows the DAC, and produces better quality reproduction. This is similar to the technique used in common oversampling audio CD players, but at MHz rather than KHz rates.

Similarly to the ADC, the DAC may provide either a single bandpass analog signal at an intermediate frequency (IF), or a pair of baseband signals which feed a quadrature mixing stage.

A fast buffer memory is needed to ensure that the DAC will receive a steady burst of data at a high rate, yet the loading of the memory can be accomplished asynchronously by one or more programmable digital computers.

The digital data for the DAC will normally have to be interpolated to translate the low-rate digital quadrature baseband data into oversampled quadrature or real data for quadrature or bandpass up-conversion respectively. Similar to the decimation discussed in section 2.3, there is a choice between performing this step using software algorithms or dedicated hardware components.

Neither software nor hardware interpolation approaches are able to match maximum required DAC data rates, so interpolation of the data will normally take more time than the output conversion for the same data.

### 2.6 Timing, Triggering and Technique Control

Precise measurement and control of receive and transmit times is important for effective counter measures. The time-of-arrival (TOA) of the pulse and PRI measurements must be exact in order to accurately schedule the time-to-transmit (TTT). This accuracy must be matched by the precision of the delay timing control that coordinates output conversion starting at the TTT. The TOA of the pulse and the TTT must be at least as accurate as the maximum radar time resolution. For ADCs operating in the GS/s range, the accuracy required for measurement and control of timing must on the order of one nanosecond.

Timing accuracies down to the nanosecond are beyond the reach of software timing loops, and will require hardware counters operating at high rates. To avoid metastable states and race conditions, great care will be needed in the design of the counters. This implies use of techniques such as gray code counters (where adjacent count values differ by only one bit), and look-ahead (as opposed to ripple) counters. These are relatively standard techniques for digital counter design. If counter techniques are insufficient, some hybrid analog/digital approach may be required whereby a precision analog ramp is digitized using an ADC. This particular approach is used in the Acqiris ADC product, described in section 3.2.

Triggering is normally associated with detection and digitization of the incoming radar pulse, but it is also important because it defines the TOA of the pulse. Triggering can be done in the analog domain using fast voltage comparators, as indicated in section 2.1. Triggering can also be done in the digital domain by operating on the data stream from the ADCs if the sampling rate is sufficiently high. This would normally require special digital hardware and digital thresholding.

In addition to the measurement of arrival times and elapsed times, there must be means provided to allow the technique control computer to control the TTT. Also, the technique control computer must be able to control the transfer of status information and technique parameters (such as filter coefficients) to the CECM processing computer(s). Such a computer must be capable of real-time operation, and would normally be dedicated to low level tasks, but no specialized technology would be necessary for this relatively low-intensity processing. The major complexity and costs associated with technique control will be in the application specific software needed to set up and control the CECM techniques.

# 3 Demonstration System and Related Performance

A demonstration system will provide the results necessary to carry the CECM concept to the next stage of development and testing. CECM could be a strong Canadian specialty in the expanding world of advanced electronic countermeasures. The following subsections deal with the objectives of a demonstration system for CECM, COTS products to meet the objectives, selection of examples of components for possible configurations of demonstration systems, upgrade path for the proposed systems and finally an analysis of estimated performance for the proposed possible systems.

## 3.1 Demonstration System Objectives

This section describes the objectives of a proof of concept demonstration system. Besides minimum target performance specified in range targets, we include desirable qualities such as future usability/expandability and maximizing use of COTS products.

We have identified six objectives for the demonstration system:

1. It must be able to jam at least one RADARSAT mode with 8 or more closely spaced range targets, each with hundreds of azimuth components
2. It should be expandable in stages for upgrades in ADCs, DACs, DSPs or other components
3. It should maximize the use of COTS products where possible
4. It should have standard interfaces and support for common development environments
5. It should be low in cost
6. It should be useable in a partial form to spread development effort and costs over time and to maintain flexibility.

Eight range targets are chosen as a minimum to demonstrate a useful number of closely spaced range targets. Using eight range targets, an image patch of eight pixels by several hundred can be achieved.

An expandable design allows a demonstration system to provide useful results at interim stages of development. By having several stages, development can progress with verifiable results that build on previous success.

Use of COTS products reduces development time, allows greater flexibility and keeps cost down.

Further, COTS products tend to be more reliable and can be more easily replaced when damaged.

Cost can be contained by purchasing hardware only as necessary for each stage since new requirements for the system may arise in the course of development. New developments in... available hardware may occur as well which we may wish to take advantage of in order to reduce cost and extend performance.

### 3.2 Selected Examples of Commercial-Off-The-Shelf Hardware

In this section we describe specific components on the market that could perform functions of each block of Figure 1. We evaluate whether each component meets requirements for an initial demonstration system only or has future use in following demonstrations or a final system. We provide only an overview of the component capabilities which are relevant for CECM.

The following paragraphs include descriptions of COTS hardware that are representative of the 'state of the art' for each CECM function at the time of writing. The investigation for this report did not include an exhaustive search, so the hardware discussed is not necessarily the best available for CECM. We believe, however, that the finding are representative of current products capabilities based on today's technology.

Acqiris is a European based manufacturer that supplies high speed ADC subsystems for the PCI bus and *compact* PCI (cPCI) bus. The PCI bus is used in most modern desktop personal computers. Acqiris supplies ADCs that can vary their sampling rates from 100 samples per second (S/s) to 2 gigasamples per second (GS/s) at 8 bits, with precise time-stamping and synchronized multi-channel cards. Planned future products will include DACs able to match Acqiris's ADCs in performance. The ADC boards have 128 kilobytes per channel onboard buffering to handle the fast data-capture rates at full speed, and can transfer data over the PCI or cPCI bus at speeds up to 100 megabytes per second (MB/s). If needed the onboard memory can be expanded to 4 megabytes. Acqiris boards feature digital triggering, over-voltage protection, programmable input voltage range scaling (useful for AGC) and programmable input impedance. All of these features are useful for a prototype or a final system. See appendix A for the Acqiris DC240 specification sheet.

Gage is a Canadian based company that manufactures PC based measurement equipment. Among their products is a DAC that can operate at up to 80 megasamples per second (MS/s). They also provide PCI based ADC boards that operate at sampling rates up to 2 GS/s. Both boards can be configured with a large range of memory sizes. Features of their ADC board are similar to those Acqiris specify for their ADC boards. Currently the DAC board is only available on the ISA bus which severely limits its data transfer rates and so its usefulness for CECM, but a PCI version is reported to be in development. The products are suitable for a demonstration system but will require a PCI bus based DAC for a final system. See appendix B for Gage's CompuScope and CompuGen products.

Celerity offers 750 MS/s ADC, DAC and memory systems on VME bus cards and can move data at 750 MB/s using their custom parallel bus system. Currently the custom interface is only supported on their ADC, DAC and a large memory card. Data movement to any other device, such as a DSP, would rely on the relatively slow VME bus or require custom interface to the parallel bus system. The use of a non standard interface and necessity for external signal thresholding and timing are undesirable for a demonstration or final system. The 750 MS/s ADC and DAC and capability of fast data movements are suitable for a demonstration or final system, but the costs are unsuitable for a demonstration system. See appendix C for a description of Celerity's GIGAFLASH750 system.

GRAY CHIP provides a line of chips for digital signal manipulation including up/down conversion, digital quadrature formation, decimation/ interpolation and digital filtering. The current line of chips include a quad channel receiver (70 MS/s in), quad channel transmitter (62.5 MHz out) and a resampler (80 MS/s in). All of these chips handle 12 bit data and allow microprocessor interface for control, data and diagnostics.

The GRAY CHIP transmitter chip allows four independent modulators and a large range of interpolation factors with 90 dB spurious free dynamic range. The receiver chip allows four independent real down-convert channels or two complex independent down-convert channels, a large set of decimation factors, and 115 dB spurious free dynamic range.

GRAY CHIP data rates are sufficient for a demonstration system but may not be adequate for a final system. The use of these products would require fabrication of a custom carrier board with interfaces. See appendix D for GRAY CHIP's digital receiver chip, GC4114.

PENTEK offers a full range of ADC, DAC and signal processing boards. They also provide a wide variety of external I/O interfaces for all of their devices. The PENTEK line of digital signal processors varies from a few million operations per second to several billion. Currently they only provide VME bus boards but are planning to provide cPCI boards by the third quarter of 2000. The ADC and DAC that PENTEK provides are in the 70 MS/s and 200 MHz ranges respectively, however they are proposing technical cooperation with Acqiris for integration of Acqiris's ADC and future DAC. The ADC and DAC bandwidths are sufficient for a demonstration system but do not meet the high bandwidth necessary for a final system. The PENTEK line of DSP boards is attractive for development since new boards can be added to the system for increased computational power. The cost of their various interfaces and wide selection of components results in premium prices.

Other signal processing equipment investigated include Motorola's Altivec processor (the "G4") and Intel Pentium processor in personal computers. The high clock speed and buffered operation of PCs allow them to compete with more common signal processing chips at much lower cost. Investigation with the CECM computations showed that a high end Intel Pentium PC running unoptimized C code can perform the core CECM signal processing 2.5 times faster than a Texas

Instruments C40 DSP with highly optimized assembly language coding. When the same C code was used on both the Intel Pentium and TI C40, the Intel chip was 50 times faster. Preliminary investigations of the core CECM signal processing C code on the G4 showed that the floating point vector handling of the Altivec versus standard floating point processors can improve performance by a minimum of 2.5 over that possible using the G4 floating point unit alone. The comparison was made on a Macintosh computer with and without the Altivec extension using the same clock frequency, cache sizes and other CPU and memory parameters. See appendix E for Motorola's Altivec processor specification overview.

The standard VME bus has a data transfer rate of 40 MB/s. Variations exist for 64 bit($VME_{64}$, double width) and higher clock speed, bringing the data transfer rate to a maximum of 160 MB/s, but these interfaces are specialized and therefore are more expensive and not widely supported. The standard PCI and cPCI buses have a data transfer rate of 100 MB/s. The PCI and cPCI use the identical standard except for the interface connector. Currently bridges between cPCI and PCI will only support a data transfer rate of 45 MB/s. Any of these busses are sufficient for a demonstration system but a final system will require a higher data transfer rate to maximize the time available for signal manipulation for high bandwidth, high duty cycle radars.

Table 1: Summary of Manufacturers' Relevant Products and Web Sites

| Manufacturer | Product | Web Site |
|---|---|---|
| Acqiris | DC240, card cage, PCI bridge | http://www.acqiris.com/ |
| Gage | CompuScope, CompuGen | http://www.gage-applied.com/ |
| Celerity | VME-ADC750, VME-DAC750 | http://www.csidaq.com/ |
| GRAY CHIP | GC4114, GC4016, GC3011 | http://www.graychip.com/ |
| Pentek | 6472-70MHz ADC | http://www.pentek.com/ |
| Altivec | G4 | http://www.altivec.org/ |

### 3.3 Example Demonstration System Configurations

This section recommends parts for two example demonstration systems and explains how the demonstration systems could meet the objectives described in section 3.1. We describe how the overall systems might be assembled, programmed and tested. We also identify the benefits and risks for the proposed approaches. This is not intended to be a detailed hardware specification, which is beyond the scope of this work.

The first example demonstration system breaks development into two stages to spread out the development and cost of the demonstration system , and to allow for incorporation of future

COTS products. The two stages build upon one another by starting with an initial system and expanding upon that system. We call the two stages the initial and expanded demonstration systems.

The initial demonstration system is based on the following hardware supported by appropriate software:

-An Acqiris DC240 dual channel DAC
-A cPCI card cage
-A cPCI to PCI bridge
-A high end PC

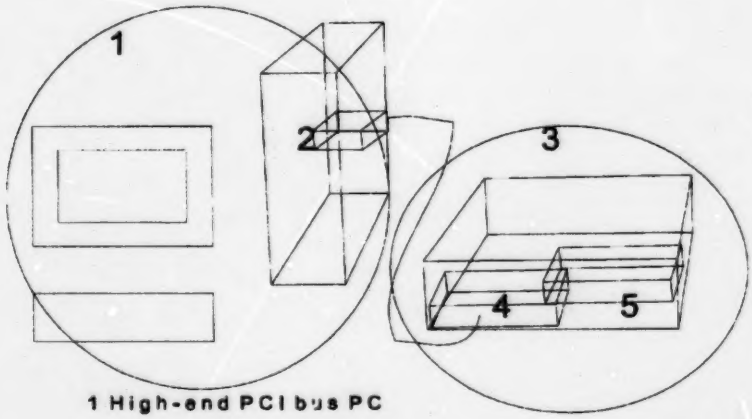


Figure 2: Initial Demonstration System Configuration

As explained above, and more thoroughly in section 3.4, the initial system will be enhanced in an additional development stage to add the DAC and timing and control subsystems. Due to data transfer rate and computation restrictions, signal sampling will be of an analog quadrature signal via two ADC channels. Since sampling speed and buffer memory are priority concerns, this example system uses the Acqiris line of ADCs. Furthermore Acqiris's handling of timing simplifies the need for customized development of timing control hardware, and their future support of a DAC synchronized to the ADC triggering makes them a good choice for the CECM application. Choosing the Acqiris products dictates that we must choose a compact PCI (cPCI)

bus.

Pentek's promise for third quarter 2000 distribution of cPCI-based line of DSP boards and other peripherals make the cPCI a reasonable choice for CECM development from the point of view of expandability and upgradability.

A standard Pentium III PC can serve a multiple role in programming, control and signal processing for the demonstration system. This necessitates the PCI to cPCI bridge which limits the data transfer speed to 45MB/s for the initial demonstration system. Testing with the CECM algorithm on several different processors has shown that there is sufficient computing power in a standard PC to perform a useful number of target calculations. If more powerful processing over the cPCI bus is added later, the PC can still be used in a final system for programming and control. A final high performance system could use several parallel dedicated high performance DSP boards for signal processing.

Risk areas for the first example demonstration system include:

-Delays in the delivery of the promised Acqiris DACs

-Timing and data transfer in a PC environment

It is difficult to predict the timing restrictions for external I/O that might arise due to the PC's general purpose design and non real-time Windows operating system. Although the CPU may have the computational power, the system overhead may impede continuous high speed data movement and sustained computation. One delay in the PC performance will be the movement of data from memory through caches to the CPU. The significance of this will need to be verified but is currently assumed to be small. The risks can be mitigated by going with a custom DAC and using a real time OS like QNX or Linux-Hard Hat.

A second possible example demonstration system configuration would be based on current Gage products and again spread development by first using a single channel for real data capture and reproduction, then expanding by adding the complexity of a second channel and faster DAC for complex quadrature sampling and reproduction.

This proposed system would use a Gage CompuScope (PCI) and a CompuGen (ISA) card for ADC and DAC cards respectively. Since Gage products are PCI based, there is no need for a cage and bridge. Currently the CompuGen is only available in ISA bus format. The ISA bus is approximately 100 times slower than PCI bus for data transfers. A PCI based CompuGen is in development but the release date is not available. The use of a single channel that is sampled only as real data would limit the types of patches produced to those that are symmetrical in azimuth. The Gage ADC is directly comparable to the Acqiris ADC for performance and features. An initial benefit is that the Gage product is PCI based rather than cPCI so the initial

transfer speeds will be the full 100MB/s achievable with PCI technology. As with the previous example system the risks are the same, failure of an adequate DAC becoming available and the unknown timing problems associated with the PC system.

Arguably a full demonstration CECM system could be built based on the VME bus. However, the limited ADC bandwidths for currently supported VME bus ADC boards would only support a development system. Furthermore, the VME bus only supports data transfer rates of 40MB/s, which would limit expandability in the critical area of data transfer bandwidth. For these reasons, a VME example is not presented here.

### 3.4 Upgrade Path

This section describes how the example demonstration systems can be expanded. It discusses additions or upgrades for the near and medium term including additions of DACs and possibly a DSP board. We show how either the initial and expanded demonstration systems from the first example or the second example fit into the proposed upgrade plan and what benefits and costs result from upgrades. We further discuss medium and long term goals for the demonstration systems and an eventual final system, and how the proposed demonstration components could be reused in the future.

VPI has developed software routines necessary for the calculation and simulation of CECM in SAR images. This work could be considered stage zero of a development series. The next stage would be to add an ADC for actual data capture and real data movement, this would be either example demonstration system specified in section 3.3. The initial Gage example system would allow limited CECM image testing with the slow ISA bus based DAC. The resolution would be limited, focus poor, and images patches restricted to be symetrical.

Once the problems of interfacing, data movement, buffering and coordinated calculation are overcome the next development stage would add a fast DAC, fast output buffer and timing and control hardware to the system. The expanded demonstration system would be capable of full field demonstration against live radars.

The initial and expanded demonstration systems support many avenues for upgrade including future additions of DSP boards for improved signal processing performance. For the Acqiris system the cPCI cage would allow future use of the 100 MB/s transfer rate of the cPCI bus when a cPCI DSP board is added for local dedicated signal processing. The cPCI to PCI bridge would still be used for programming and monitoring via the Pentium PC but no longer used for extensive data movement. Pentek's proposed technical cooperation with Acqiris and promised support of cPCI provides a future line of COTS upgradable products. The Gage system can be expanded to include a second channel and PCI DAC for faster data transfer. The second channel would allow asymmetrical image patches and wider bandwidths of signal reception and transmission. The PCI DAC would allow much greater data movement bandwidth allowing

more time for computation. Further improvements could be realized by simply purchasing the next generation PC processor for improved calculation performance or a PCI based DSP. By using a Pentium PC and development under the C language, the software development should proceed rapidly and should port to future processors with relative ease[4]. Either ADC, if eventually replaced, is still usable as a high performance digital oscilloscope that may be used for monitoring in the system or for other purposes.

### 3.5 Performance Predictions for the Expanded Demonstration Systems

In this section we list specific scenarios/radars that the Acqiris expanded system and the Gage initial and expanded systems might counter, and estimate the expected levels of performance expressed in number of range targets against each radar. The estimated levels of performance against specific radars for the example demonstration systems are presented in Table 2 and 3, and are based on the time line of Figure 3 below. Note that the results for the Acqiris system assumes use of the cPCI to PCI bridge and use of a Pentium computer, while the Gage system assumes use of the PCI bus and Pentium computer. Both sets of results assume a suitable high speed DAC is available for the expanded version of each example demonstration system.

[4] Intel based PCs are the most popular environment for cross compatibility of C code to a wide variety of processors.

Table 2: Estimated Performance of Acqiris Expanded System For Specified Radars

| RADAR | Modes | Radar parameters | | | Estimated number of full resolution range targets |
|---|---|---|---|---|---|
| | | BW (MHz) | PW (μs) | PRF (Hz) | |
| RADARSAT1 and common RADARSAT2 modes | Fine modes | 30 | 42 | 1400 | 4 |
| | Standard modes 1 and 2 | 17.28 | 42 | 1400 | 9 |
| | Wide modes and S3 - S7 | 11.58 | 42 | 1400 | 15 |
| RADARSAT2 other modes | GMTI | 50 | 42 | 2500 | Nil |
| | Additional Fine modes | 100 | 42 | 3800 | Nil |
| CCRS Convair-580 | C-band high resolution | 26.35 | 7 | 383 | 174 |
| | C-band low resolution | 8.3 | 8 | 383 | 483* |
| | X-band high resolution | 26.35 | 15 | 383 | 80 |
| | X-band low resolution | 8.3 | 30 | 383 | 127 |
| E-SAR | Narrow mode | 90 | 4.98 | 1238 | 20 |
| | Wide mode | 50 | 4.98 | 1238 | 38 |
| | Super Wide mode | 18 | 4.98 | 1238 | 109* |
| ERS-1,2 | SAR mode | 15.5 | 37.12 | 1720 | 9 |
| SIR-C | Maximum operation | 40 | 33.8 | 1736 | 3 |
| X-SAR | High resolution | 20 | 40 | 1736 | 6 |
| | Low resolution | 10 | 40 | 1736 | 14 |
| PHARUS | Typical operation | 100 | 12.8 | 2500 | 1 |
| | Maximum operation | 100 | 25.6 | 5000 | Nil |
| Pulsed Doppler Search Radar | MPRF search mode | 1 | 13 | 27000 | 30* |
| | HPRF search mode | 1 | 1.9 | 190000 | 21* |

* Assumption 5 breaks down for these cases and required deeper analysis (assumptions are described in later paragraphs). The value in the table is the refined estimate calculated without relying upon assumption 5 on page 24.

Table 3: Estimated Performance of Gage Initial and Expanded Systems For Specified Radars

| RADAR | Modes | Radar parameters | | | Estimated number of full resolution range targets | |
|---|---|---|---|---|---|---|
| | | BW (MHz) | PW (μs) | PRF (Hz) | Initial | Expanded |
| RADARSAT1 and common RADARSAT2 modes | Fine modes | 30 | 42 | 1400 | Nil | 5 |
| | Standard modes 1 and 2 | 17.28 | 42 | 1400 | Nil | 10 |
| | Wide modes and S3 - S7 | 11.58 | 42 | 1400 | Nil | 16 |
| RADARSAT2 other modes | GMTI | 50 | 42 | 2500 | Nil | 1 |
| | Additional Fine modes | 100 | 42 | 3800 | Nil | Nil |
| CCRS Convair-580 | C-band high resolution | 26.35 | 7 | 383 | 130* | 175* |
| | C-band low resolution | 8.3 | 8 | 383 | 380* | 487* |
| | X-band high resolution | 26.35 | 15 | 383 | 43* | 81 |
| | X-band low resolution | 8.3 | 30 | 383 | 87* | 128 |
| E-SAR | Narrow mode | 90 | 4.98 | 1238 | Nil | 21 |
| | Wide mode | 50 | 4.98 | 1238 | 2 | 39 |
| | Super Wide mode | 18 | 4.98 | 1238 | 65* | 110* |
| ERS-1,2 | SAR mode | 15.5 | 37.12 | 1720 | Nil | 11 |
| SIR-C | Maximum operation | 40 | 33.8 | 1736 | Nil | 4 |
| X-SAR | High resolution | 20 | 40 | 1736 | Nil | 7 |
| | Low resolution | 10 | 40 | 1736 | Nil | 16 |
| PHARUS | Typical operation | 100 | 12.8 | 2500 | Nil | 3 |
| | Maximum operation | 100 | 25.6 | 5000 | Nil | Nil |
| Pulsed Doppler Search Radar | MPRF search mode | 1 | 13 | 27000 | Nil | 33 |
| | HPRF search mode | 1 | 1.9 | 190000 | Nil | 27* |

Note that the expanded demonstration systems exceed the minimum requirement of 8 range targets in at least one RADARSAT mode by allowing 9 or more range targets in all the standard and wide modes of RADARSAT. With these systems it would be possible to generate hundreds of closely spaced range targets for some modes of the CCRS's airborne SAR. The high resolution PHARUS airborne SAR is difficult or impossible for the demonstration systems to

jam due to the large data volume that must be transferred internally for CECM. The large data volume is due to the high bandwidth and long pulse width of PHARUS. Also, the initial Gage system is only capable of countering the CCRS's airborne SAR with this type of performance analysis.

Our performance analysis of the example demonstration systems for CECM started with a time line as shown in Figure 3. This figure assumes each time line element occurs sequentially with no overlap in order to arrive at a conservative estimate of performance[5]. The *pulse repetition interval* (PRI) is the time between the TOA of one pulse and the TOA of the next pulse. A demonstration system must modify every pulse, therefore it must complete all necessary operations to modify a pulse within the PRI[6]. The time it takes to sample the pulse is the *pulse width* (PW). The PRI minus the PW is the time available for moving the buffered captured data to a memory for processing, processing the data and moving the data out of working memory to a buffer for transmission. Note that digital to analog conversion is assumed to proceed in parallel with the other processes.

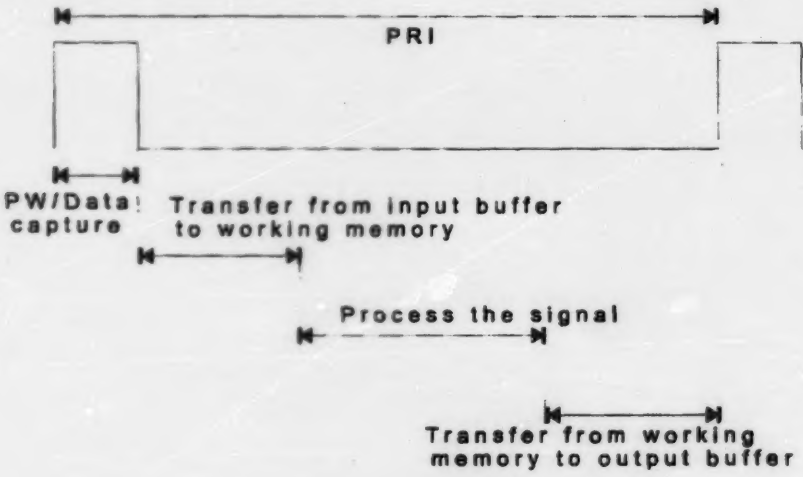
PRI
PW/Data capture
Transfer from input buffer to working memory
Process the signal
Transfer from working memory to output buffer

Figure 3: CECM Signal Handling Time Line

5 Some implementations could allow overlap of data movement and processing.

6 Strictly speaking, it would also be possible to take N PRI's to process the result if N parallel processes were set up to run in a staggered pipeline fashion to produce a result at each PRI.

The following assumptions were made to generate the results of Table 2 and 3:

1. The complex quadrature sampling rate exceeds the radar bandwidth by a factor of 1.5
2. The input data is ready for transfer at the end of the PW
3. The cPCI to PCI bridge can reach 90% of its quoted performance
4. A high end Pentium PC can achieve 150 million effective operations per second (EOPS)
5. The number of range targets compared to number of samples is small (this assumption was excluded for results shown with an asterisk)

Quadrature sampling with two ADCs at a rate to exceed the bandwidth of the radar by a factor of 1.5 surpasses the Nyquist minimum requirement by 50%, which allows for small variations in the radar timing and gives a more robust set of data for processing.

Previous testing with the CECM algorithm suggests that 150 million EOPS is reasonable to assume with a high end Pentium class machine.

See Appendix E for a description of the calculation used for determining the estimated performance of the demonstration system against specific radars.

## Conclusions and Recommendations

The primary challenge in an implementation of a CECM-capable jammer is data transfer bandwidth for digital data between the internal components of the system. Other challenges are availability of a suitable COTS DAC and the need to develop a custom timing and control system, though fortunately the timing and control system would be similar to the existing Techniques Generator of the CARDS jammer system.

Some general conclusions on CECM implementation can be summarized as follows:

1) Eight bits provides sufficient dynamic range for spaceborne SARs and most airborne SARs;
2) Current technology for CECM is not limited by computation but rather by data movement bandwidths;
3) A low cost demonstration system is possible using a PC for computation;
4) The example expanded systems can produce 9+ closely spaced range targets in RADARSAT and 100's of range targets for some airborne SARs;
5) Refinements to the example system models may include a cPCI or PCI-based data processor for higher data transfer BW, and time overlap of data processing with data transfers.

Rather than proceeding directly to a full featured CECM system, a demonstration system should be built up in two stages. First, an initial wideband intercept system should be built based on COTS components, with possible limited analog output. Second, an expanded version of the initial system should be built and enhanced with a timing and control unit and an full analog output capability using components to be determined.

The initial demonstration system might be built using an Acqiris ADC or a Gage ADC, and a low cost Intel Pentium based personal computer. The Acqiris ADC would require use of a cPCI card cage and a cPCI to PCI bridge. The initial system is sufficient to demonstrate capture of very wide bandwidth radar pulses in real time, and processing of these pulses in both real-time and slower-than-real-time. Additionally the system could have limited output for initial testing and some types of image patches. The benefits of the initial system are the ability to gain experience with the front end, refinement of requirements for timing and control, and development and testing of reusable software that can be adapted for the expanded version and for an eventual full-featured laboratory system.

The expanded system would include a dual channel wideband DAC component (COTS TBD or semi-custom board on either the cPCI or PCI bus), a custom timing and control unit, and possible "glue" and diagnostic components as required. The expanded system would be sufficient to demonstrate live CECM against medium resolution synthetic aperture radar systems such as ERS, RADARSAT, and the CV-580 airborne SAR. We estimate that from tens to hundreds of range targets (each with hundreds of azimuth components) are possible against such systems

depending on the particulars of the radar and the detailed design and construction of the CECM hardware and software.

It is recommended that a full specification of requirements be made and a deeper analysis of system feasibility be performed. This report makes many assumptions of system performance from general sources of information. The assumptions made for performance estimation should be confirmed and retired for accuracy and effect on performance. A deeper analysis would identify possibly other unforseen limitations and identify areas of improvement in performance and reduction of development risk.

## References

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[5] http://www.graychip.com/

[6] http://www.acqiris.com/

[7] http://www.gage-applied.com/

[8] http://www.csidaq.com/

[9] http://www.gage-applied.com/

[10] http://utopia.tno.nl/instit/fel/div4/pharus/pharus_home.html (10 Dec. 1999)

[11] http://www.ti.com/

[12] http://www.altivec.org/

[13] http://www.pentek.com/

[14] http://radarsat.mda.ca/

## Appendix A- Acqiris dual channel ADC specification sheet

acqiris

## Main Features

- **2 GS/s Sampling Rate (Simultaneous on 2 Channels)**
- **500 MHz Bandwidth**
- **256 kpoints Acquisition Memory per Channel (4 Mpoints optional)**
- **Memory Battery Backup Option**
- **Up to 14 Channels in One 8 Slot Crate**
- **Full Front-end Amplification with Internal Calibration**
- **50Ω and 1MΩ Input Impedance**
- **< ±1% DC Accuracy for Precise Voltage Measurement**
- **Mezzanine Front-end with Input Protection**
- **Complete Pre and Post Triggering**
- **±2 ppm Clock Accuracy**
- **Built-in 5 ps Trigger Time Interpolator (TTI) for Accurate Timing Measurements**
- **Low dead-time (<500 ns) Sequential Recording with Time Stamps**
- **1 GHz Auto-Synchronization-Bus (ASBus) for Trigger and Clock Signal Distribution**
- **Modular, 6U CompactPCI**
- **Low Power (<40 W)**
- **AcqirisLive Software for Windows Complete with Source Code Examples**
- **"Plug & Play" Installation**
- **National Instruments LabVIEW and LabWindows/CVI Drivers**
- **Very high Data Transfer Rate to Host PC**

## High Frequency Waveform Recording

**High Speed and Precision** - The Model DC240 Digitizer sets new standards in CompactPCI/PXI based data acquisition. The digitizer features two input channels, each with fast sampling rate (up to 2 GS/s), 8 bit resolution, wide bandwidth (500 MHz) and long 256 kpoints acquisition memory (optional to 4 Mpoints). The fast sampling rate and wide bandwidth combine to allow the accurate capture of signals up to 500 MHz in frequency.

Waveforms are stored directly into the digitizer's large acquisition memories enabling complex signals to be acquired over very long time periods. Only large memories allow digitizers to maintain fast sampling rates (and therefore high timing resolution) over long time periods. For example, a Model DC240 with 4 Mpoints of memory can record a signal over a 2 ms period with a sampling rate of 2 GS/s (0.5 ns per point). The fast sampling rate ensures all high frequency signal components, up to the full bandwidth (500 MHz) of the digitizer, are accurately recorded. If the memory was reduced to 20 kpoints the sampling rate would have to fall to just 10 MS/s (20,000 points / 2 ms). Frequencies above 5 MHz would then be incorrectly digitized and important events may be missed completely. The Model DC240 delivers high-speed performance, over long time periods, without compromising on acquisition memory or signal quality.

**Up to 14 Channels in One Crate** - The Model DC240 is a dual CompactPCI/PXI (6U) module that is ideal for use in multi-channel applications. For example, a single 8-slot 6U PXI crate (CC108) can house up to 7 modules (plus an interface) to make an 14 channel bench-top data acquisition system. The low power consumption of the DC240 (typically 40 W) results in an 14 channel system that uses the same power than most comparable 4 channel bench-top oscilloscopes. For high-density rack mounted applications multiple crates can even be daisy-chained. This makes it possible to build a system containing hundreds of channels of data acquisition that is totally controlled over a single bus!

The Model DC240 includes Acqiris' ASBus, a proprietary high bandwidth auto-synchronous bus system. In multi-channel applications, ASBus is a vital tool that takes care of the distribution of all necessary trigger and clock signals. The system improves trigger flexibility by allowing any modules input to be used as the trigger source for all the digitizers. For synchronous data acquisition, ASBus allows all the digitizers to be clocked at precisely the same time. Synchronous digitizing improves the accuracy of cross-channel measurements and is essential for accurate time correlation. The ASBus can also be used to phase-synchronize all the digitizers to an external standard (such as a 10 MHz reference).

**PC Control and Convenience** – Using a DC240 Digitizer is just like driving a familiar digital oscilloscope. Windows based software allows adjustment of the key acquisition settings such as time-base, trigger and sensitivity while state-of-the-art front-end electronics enables high fidelity recording with full control over features such as input impedance, coupling, gain and offset. Data recorded by the DC240 can be transferred directly to a host PC at rates up to 100 Mbytes/s. Combining the fast transfer rates with today's most powerful PC processors makes it possible to perform measurements and calculations hundreds of times faster than with conventional instruments.

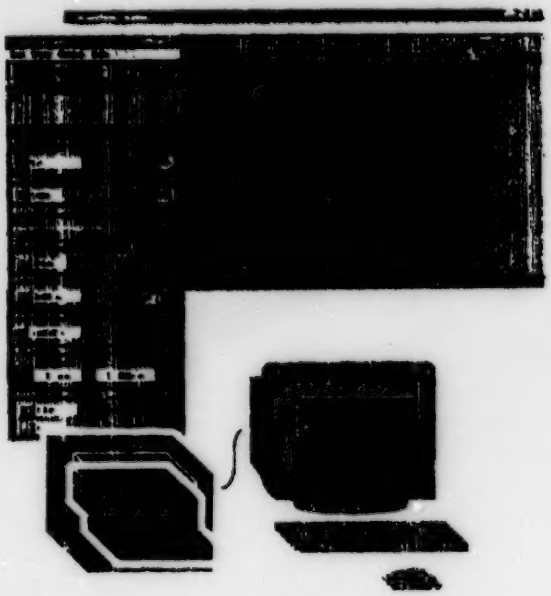
You can also store hundreds of waveforms directly on the PC's hard disc or make hard copies instantly on your printer. Archiving important waveforms has never been easier. Furthermore, you can interface directly to your desktop PC and use the Internet (or a local network) to send important information to others anywhere and at anytime. The result is flexibility and performance that can dramatically reduce testing times, increase measurement throughput and lower overall cost. For high-frequency applications (up to 500 MHz) in Telecommunications, Magnetic Media, Automotive, Time of Flight Mass Spectroscopy, Computing, Particle Physics, Military, Explosive-Weapons and Ballistic Testing, the DC240 is the digitizer of choice.

## Scope Like Characteristics: Amplifier, Trigger and Time Base

**Mezzanine Front-end** - The signal input of each DC240 Digitizer has programmable front-end electronics that provides a complete set of input voltage ranges (from 50 mV to 5 V full scale in a 1, 2, 5 sequence) and variable voltage offset. The inputs have selectable impedance (50 W or 1 MW) and are fully protected against over-voltage signals. The amplifiers feature internal calibration (no need to disconnect input signals) and fast recovery from out-of-range signals. The input buffer is mounted on a removable mezzanine card so, in the event of accidental damage or as components fatigue over time (e.g. relays in high duty cycle automated testing applications), replacement is fast and efficient.

**Flexible Trigger** - The digitizers include a precision trigger system with full pre and post trigger adjustment. User selectable coupling is combined with internal or external trigger sources for maximum flexibility. The digitizers also provide a sophisticated sequential trigger mode with less than 500 ns dead time between successive triggers. This extremely low dead time enables events, which may occur at very high repetition rates, to be captured and stored in their correct arrival sequence. This trigger mode is perfect for "impulse-response" type applications (RADAR, SONAR, LIDAR, Time-of-Flight, Ultrasonic, Medical & Biomedical research, etc.). The sequential trigger mode and very low dead time greatly extend the digitizers timing range and resolution. Each event can be individually time stamped and relative time measurements (between events) can be made with less than 1 ns resolution.

**Precision Time Base** - Each digitizer also has its own crystal-controlled precision time base better than ± 0.0002% accuracy. The high accuracy improves measurement precision and is extremely important when working with complex signals that are recorded over long time periods. Sample rates can be selected, in a 1, 2, 2.5, 4, 5 sequence, from 100 S/s to 2 GS/s. An internal Trigger Time Interpolator (TTI) with high timing resolution is used to assist with timing calibration and trigger positioning. The TTI permits accurate positioning of the trigger signal with regards to the internal clock (sampling time). The sample rate can also be generated externally, using the external input connector, for applications where the sample rate must be synchronized with the signal to be acquired.



*Modular CompactPCI 6U System*

## Appendix B- Gage's CompuScope and CompuGen specification sheets

# CompuScope 8500

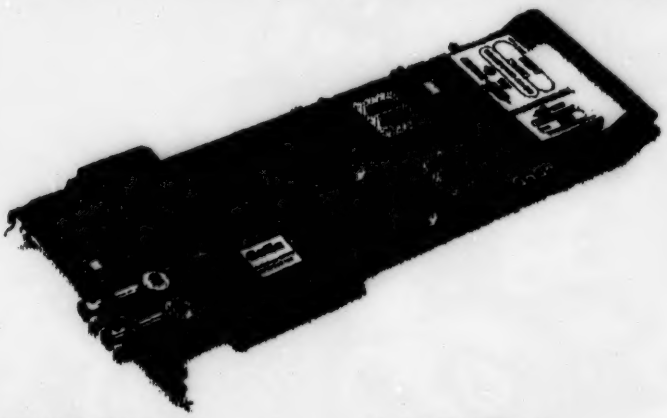
**World's fastest A/D**

CompuScope 8500 is a

These cards provide the

for the PCI Bus.

high speeds.



## COMPUSCOPE 8500

CompuScope 8500 can sample one analog input at speeds up to 500 MS/s with 8 bit resolution and either store the data in the on-board memory or read it directly into the PC's memory at rates up to 100 MS/s.

## 500 MS/S SAMPLING

The CS8500 uses a high-quality flash A/D converter which can digitize at 500 MS/s rate. In other words, a new sample is taken every 2 nanoseconds.

An on-board crystal-controlled timing circuit ensures timebase accuracy and long-term thermal stability of CompuScope 8500.

## 1 MΩ AND 50 Ω INPUTS

In order to maximize the capabilities of the CompuScope 8500, two separate inputs have been provided and the user has the ability to select between the two.

The first input has 50 Ω input impedance and provides very high bandwidth. No input protection is provided for this input and the user must ensure that the amplifiers are not overdriven.

The second input has 1 MΩ input impedance compatible with all standard scope probes. This input has on-board input protection circuitry and a 100 MHz bandwidth.

## DIRECT A/D INPUT OPTION

Finally, the user also has the option to bypass the analog front-end of the CompuScope 8500 and input a signal directly into the A/D.

The advantage of inputting the signal directly into the A/D is that the bandwidth can be maximized and distortion minimized.

Care must be taken not to overdrive the signal in this mode, as that can irreparably damage the A/D chip. Also note that when the Direct A/D Input Option is installed, the 50 Ω and 1 MΩ inputs are no longer available.

## MEMORY DEPTH

CompuScope 8500 is available with memory depth from 2 MB to 16 MB.

The on-board memory can be used as a circular buffer for storage of pre- and post-trigger data.

The maximum number of sample points which the CompuScope 8500 can capture is equal to the memory depth of the model being used; for example, the 2 MB model can store 2 megasamples of data.

The data stored in the CompuScope 8500 memory can be transferred to the PC memory or hard disk for post processing without any interface bus (no GPIB or IEEE 488 bus required).

## 100 MB/S BUS THROUGHPUT

The high-speed, 32 bit, bus-mastering interface to the PCI bus allows the data from the on-board memory of the CompuScope 8500 to be transferred to the PC memory, or any other PCI destination, at rates up to 100 MB/s under single-tasking operating systems such as MS-DOS. Under Windows 95/98 or NT, this rate depends on the architecture of the user application. Under controlled conditions, it is still possible to achieve 100 MB/s recording speed to the PC's host memory or an MMD-5400 memory board.

## RECOMMENDED MOTHERBOARDS

All benchmarks have been made using the N440BX motherboard from Intel Corporation.

This motherboard uses the TRITON BX chipset which is recommended for use with the CompuScope 8500 if the optimum transfer rates are required.

PCI Motherboards or CPU cards designed around chipsets other than Triton BX are also compatible with the CompuScope 8500, but may not provide the same data throughput.

## BUS MASTERING

CompuScope 8500 is fully capable of becoming a PCI bus master in order to transfer data at the maximum rate of 100 MB/s.

A PCI bus Master is a card which can take control of the bus and transfer data to any PCI target device such as system RAM, a DSP card, etc., without any involvement from the CPU.

When a PCI card such as the CompuScope 8500 becomes the bus master, it is said to be operating in the Master Mode.

On the other hand, when the CPU is controlling the transfer of data from the add-on card to its system RAM, the card is said to be working in the Slave mode.

According to benchmarks carried out by Gage, the maximum throughput possible in the Slave mode of operation is approximately 10 MB/s, less than one-tenth of the Master Mode.

## FLEXIBLE TRIGGERING

CompuScope 8500 features state-of-the-art analog triggering.

An analog comparator provides triggering from the input channel, from an external signal or from software.

In addition to the trigger source, trigger level and slope are also selectable by software, making the trigger system similar to traditional oscilloscopes.

### COMPUSCOPE 8500 FEATURES

- 500 MS/s Real-time A/D
- 32 Bit PCI Bus Interface
- 8 Bit Resolution
- Up to 16MB Memory Buffer
- 100 MB/s Data Transfer Rate to PC Memory
- Optional Real-time Capture to PC Memory at 100 MS/s
- 250 MHz Bandwidth
- 40.5 dB SNR

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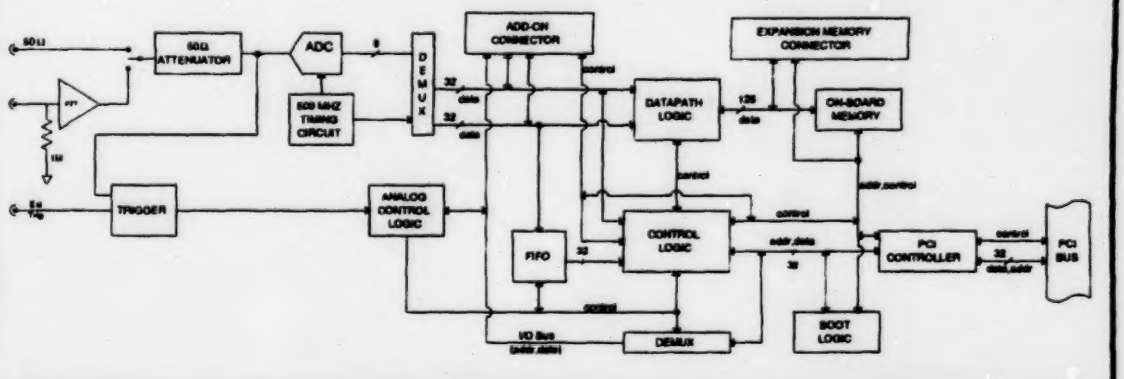
# CompuScope 8500 Block Diagram




## OPTIONAL REAL TIME MODE

A Real Time Mode upgrade can be ordered from the factory which allows the data stream generated by the ADC chips to be streamed to host memory without any breaks in data conversion. This is made possible by an on-board FIFO which accommodates PCI bus latencies.

Real Time mode is currently only supported under the MS-DOS operating system. Windows drivers do not support real time mode due to the multi-tasking nature of Windows and due to non-deterministic interrupt latencies under Windows.

## FREE GAGESCOPE FOR DOS DIGITAL OSCILLOSCOPE SOFTWARE

CompuScope 8500 is accompanied by a free copy of the powerful, full-color GageScope for DOS software which allows the computer housing the CompuScope 8500 to emulate a Digital Oscilloscope.

Users can capture data, display it on the screen, print the data, load and store data and setups, use cursors to make measurements and perform FFT and other mathematical functions.

GageScope for DOS can also be used by an engineer to verify if the CompuScope 8500 meets his or her needs before committing to writing customized software.

In other words, GageScope for DOS minimizes the development risk for users who must write their own program.

## SOFTWARE SUPPORT

Gage's OEM Support Program offers qualified developers and OEMs the support to make CompuScope 8500 a part of their products.

CompuScope 8500 belongs to a class of Gage boards called CP500. All these boards are supported by a common driver and Software Development Kit (SDK). Hence, the SDK which supports CompuScope 8500 is the CP500 SDK. For example, the SDK for Windows NT for CompuScope 8500 is called CP500 SDK for Win NT.

SDKs for Windows 95/98, Windows NT and DOS can be purchased. SDKs include driver disks, sample source code in C/C++, and detailed reference manuals.

SDKs for third-party packages such as MATLAB and LabVIEW are also available.

The SDK for DOS consists of source code routines in C. Sample programs are provided in Borland C and Watcom C. A detailed reference manual is also provided.

## GATED DIGITIZATION OPTION

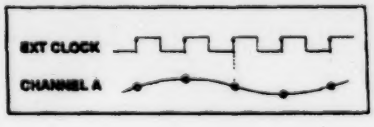
A Gated Digitization option can be ordered from the factory. Data is stored in the RAM only when the external TTL GATE input is HIGH.

This can be useful when it is desirable to stack successive data captures in the on-board memory.

## EXTERNAL CLOCK OPTION

An external clock option can be ordered from the factory in situations where a special real-time sampling frequency is desirable or when the digitization must be coherent with the rest of the system.

A new sample is taken on every rising edge of the clock.




The user is responsible for ensuring that the external clock frequency remains higher than 200 MHz and lower than 500 MHz.

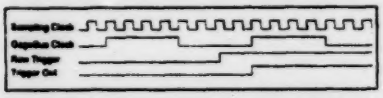
It is preferable if the external clock supplied is a differential ECL signal.

## TRIGGER OUT MODIFICATION

Trigger Out Modification on CompuScope 8500 provides a TTL output signal which signifies whether a trigger event has occurred or not.

This is useful in applications which require external devices to be synchronized or initialized at the same time as the trigger on the CompuScope 8500.

Trigger Out signal is synchronized to the GageBus clock, an internal clock signal on the CompuScope 8500 which runs at one-eighth the frequency of the sampling clock.



GageBus clock is used for storing data in on-board memory after demultiplexing the high speed data coming out of the ultra-fast A/D on the CompuScope 8500.

Triggering external devices such as ultrasonic pulser-receivers or radar signal sources allow the entire system to work synchronously with the internal GageBus clock, thereby synchronizing the rest of the system to on-board memory storage.

## MULTIPLE RECORD

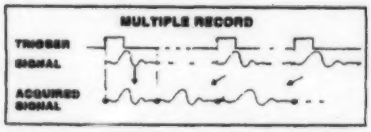
Even though the PCI bus allows very fast data throughput to PC memory, there may still be applications in which data bursts cannot be off-loaded either because of very fast trigger repeat frequency or because of software limitations.

Multiple Recording allows CompuScope 8500 to capture data on successive triggers and stack it in the on-board memory (Memory Mode) or stream it to a buffer in the PC's memory (Real-time Mode).

Capturing pre-trigger data is an optional upgrade, while post-trigger data is a standard feature on CompuScope 8500.

GageScope software can display the stacked data as individual acquisitions. Software drivers also provide support for accessing Multiple Record data.

Once the CompuScope 8500 has finished capturing a Multiple Record segment, the trigger circuitry is automatically re-armed within 16 sample clock cycles to start looking for the next trigger. No software intervention is required.




It should be noted that Multiple Recording in the Real-time Mode will work only if the sample rate is less than 100 MS/s.

Unlike the ISA bus CompuScopes, Multiple Recording on the CompuScope 8500 supports pre-trigger data, as an optional feature. Post-trigger data Multiple Record is a standard feature. The record length in Multiple Record mode can be specified with a 128 point resolution. The minimum record length is 256 points.

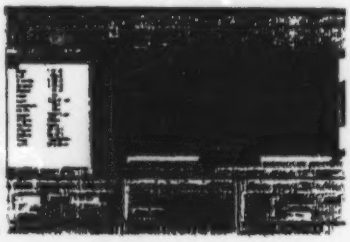
Multiple Recording is useful for applications in which a series of bursts of data have to be captured in quick succession and there is not enough time to off-load the data to the PC memory. Another situation in which Multiple Recording may be used is when data storage has to be optimized. These are cases in which only certain portions of the incoming signal are of interest and data capture during the dead-time between successive portions is not useful. Examples of these situations are radar pulses, ultrasound data, lightning pulses, imaging signals and explosion data.

## APPLICATIONS

Digital Oscilloscope
Ultrasonic Testing
Laser Doppler Anemometer
Laser Diode Characterization
Lidar
Non-Destructive Testing
Ultrasonic Materials Testing
Disk Drive Testing
Acoustic Emission Testing
Radar Signal Analysis
Telephony
Explosion Testing
Spectrum Analysis
Vibration Analysis
Nuclear Instrumentation
Ultrasonic Imaging
High-End Video Testing
Automotive Ignition Testing

## GageScope for Windows

### WORLD'S MOST POWERFUL OSCILLOSCOPE SOFTWARE



GageScope for Windows is a solutions-oriented software package allowing you to control all parameters of CompuScope cards with the click of a mouse – plus view and analyze the captured signals using the power of a Pentium processor and Microsoft Windows.

GageScope for Windows not only captures data using CompuScopes, it can also analyze the data and automatically calculate the result, which is displayed in InfoView.

An infinite number of signals and setups can be saved using GageScope for Windows. Saving signal files allows you to post-process the data from within your own software. Signal files can also be read by analysis packages such as MATLAB.

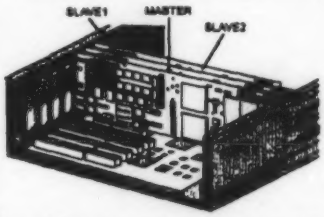
The SuperRes Mode in GageScope for Windows allows you to enhance the effective resolution well beyond 24 bits using proprietary oversampling techniques and built-in signal processing.

Powerful Plug-Ins for GageScope for Windows are also available, including:

- FFT Plug-in for spectral analysis – with up to 1 Million Point FFTs possible
- Waveform Parameters Plug-in – automatically measure and display Rise Time, Fall Time, Pulse Width, Frequency, Amplitude and many other parameters
- AutoSave Plug-in – save transient signals to disk with time and date stamp. Save both pre- and post-trigger data
- Averaging Plug-in – average virtually unlimited acquisitions to cancel random noise. Co-adding is also available
- Master Slave Plug-in – controls up to 16 channel oscilloscopes

GageScope for Windows can be ordered from the factory. Please see the specification sheet on GageScope for Windows for more detailed information.

## MULTI-CARD SYSTEMS




One of the most unique features of the CompuScope cards is the Multi-Card system that can be configured.

A Multi-Card system, comprised of one Master and up to 7 Slave boards, can be ordered from the factory if the user wants to capture more than one channel with a common clock and trigger. A board-to-board interconnect will be supplied with the system. This interconnect carries all the signals needed for proper synchronization.

GageScope Multi-Card software can then display all channels from these boards on the same screen. Software drivers also support such Master/Slave systems.

Another class of Multi-Card systems is the Multiple/Independent type. A Multiple/Independent system does not have common clock and triggering but can consist of CompuScope boards of different types and memory depths. For example, a CompuScope 8500 can be used with a 12 bit CompuScope card.

## ORDERING INFORMATION

### Hardware & Upgrades

| | |
|---|---|
| CompuScope 8500-2M | 850-181-003 |
| CompuScope 8500-8M | 850-181-005 |
| CompuScope 8500-16M | 850-181-006 |
| 2M to 8M Upgrade | 850-181-014 |
| 2M to 16M Upgrade | 850-181-022 |
| 8M to 16M Upgrade | 850-181-023 |
| External Clock Upgrade | 850-181-005 |
| Gated Digitization Upgrade | 850-181-004 |
| Master Multi-Card Upgrade | 850-181-006 |
| Slave Multi-Card Upgrade | 850-181-007 |
| Master/Slave Timing Module | 850-181-018 |
| Trigger Out Modification | 850-181-016 |
| MULREC Trigger Out Upgrade | 850-181-027 |
| Real Time Mode Upgrade | 850-181-024 |
| Direct to ADC Input Upgrade | 850-181-025 |
| GageBus Clock Out Upgrade | 850-181-026 |
| Periodic Re-Calibration | 850-181-008 |
| X10/X1 Probe (High Bandwidth) | 220-100-003 |
| X100 Probe | 220-100-002 |

### GageScope for Windows Software

| | |
|---|---|
| GageScope for Windows | 200-100-001 |
| GSWin: Master/Slave Plug-In | 200-100-002 |
| GSWin: Waveform Parameters | 200-100-003 |
| GSWin: FFT Plug-In | 200-100-004 |
| GSWin: AutoSave Plug-In | 200-100-005 |
| GSWin: Averaging Plug-In | 200-100-006 |

### Software Development Kits (SDKs)

| | |
|---|---|
| Gage SDK & Driver Pack on CD | 200-113-000 |
| CP500 SDK for Win NT | 850-113-005 |
| CP500 SDK for Win 95/98 | 850-113-004 |
| CP500 SDK for DOS | 850-113-001 |
| CP500 SDK for MATLAB Win NT | 850-113-015 |
| CP500 SDK for MATLAB Win 95/98 | 850-113-014 |
| CP500 SDK for LabVIEW Win NT | 850-113-010 |
| CP500 SDK for LabVIEW Win 95/98 | 850-113-009 |

*All Upgrades performed at the factory*

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# COMPUSCOPE 8500 SPECIFICATIONS

## SYSTEM REQUIREMENTS

PCI-based IBM compatible with 1 free full-length PCI slot. 600K conventional RAM (620K for Multi-Card), 3 MB free hard disk space and VGA graphics recommended.

## SIZE

Single-slot full-length PCI board, 13" x 4.1"

## POWER

| | Worst Case | Typical | Power Down |
|---|---|---|---|
| + 5V | 25 W | 15 W | 10 W |
| +12V | 20 W | 15 W | 0.1 W |
| -12V | 1 W | 0.6 W | 0.6 W |

## A/D SAMPLING

Number of Inputs: 1

Sampling Rate: MS/s: 500, 250, 200, 125, 100, 50, 25

Resolution: 8 bits

Aperture jitter: 2 ps, rms

Sampling Clock: Crystal controlled

## 50Ω INPUT CHANNEL

Connector: SMA

Impedance: 50Ω

Coupling: DC only

Bandwidth:

| Input Range | Typical Bandwidth |
|---|---|
| ±500mV, ±1V | 250 MHz |
| ±2V, ±5V | 250 MHz |
| ±200mV, ±100mV | 90 MHz |

Voltage Range: ±100mV, ±200mV, ±500mV, ±1V, ±2V, ±5V

Absolute Max. Amplitude: ±6 Volts continuous

DC Accuracy: ± 2 %

SNR: 40.5 dB @ 500 MS/s 1.88 MHz input in ±1V range

## 1 MΩ INPUT CHANNEL

Connector: BNC

Impedance: 1 MΩ, 25 pF

Coupling: AC or DC

Bandwidth:

| Input Range | Typical Bandwidth |
|---|---|
| ±4V | 75 MHz |
| ±2V, ±1V | 100 MHz |
| ±400mV, ±200mV | 90 MHz |

Voltage Range: ±200mV, ±400mV, ±1V, ±2V, ±4V

Input Protection: Diode Clamped

Absolute Max. Amplitude: ±15 Volts

DC Accuracy: ±2 % of full scale

SNR: 40.5 dB @ 500 MS/s 10 MHz input in ±1V range

## MEMORY MODE OPERATION

Data Storage: In on-board memory

Max. On-board Memory Size: 2M, 8M, 16M

## MULTIPLE RECORD

Record Length: 256 points minimum. Can be defined with a 128 point resolution

Pre-Trigger Data: Optional feature; contact factory for availability

Post-Trigger Data: Standard feature

## TRIGGERING

Source: Input Channel, Ext Trigger or Software

Type: Analog triggering

Trigger Level: Controlled by on-board 8 bit DAC, i.e. 256 levels

Slope: Positive or Negative

Mode: Pre-, Mid-, Post-trigger

Post-Trigger Depth: 256 points minimum. Can be defined with a 128 point resolution

## EXTERNAL TRIGGER

Impedance: 1 MΩ, 30 pF

Amplitude: Absolute Max ±15 Volts

Voltage Range: ±1 V and ±5 V

Coupling: AC or DC

Bandwidth: 100 MHz

Connector: BNC

## EXTERNAL CLOCK (OPTIONAL)

Note that when this option has been performed, the only valid internal sampling rates are 500 MS/s, 250 MS/s and 125 MS/s. The following internal sampling rates are no longer valid: 200 MS/s, 100 MS/s, 50 MS/s, 25 MS/s.)

Max. Freq.: 500 MHz

Min. Freq.: 200 MHz (for lower Min. Freq., call Factory)

Impedance: 50Ω to GND

Coupling: AC

Signal Level: ECL, sine wave 0.5V rms min.

Int. or Ext. Clock: Software Controlled

## GATED DIGITIZATION (OPTIONAL)

Allows the user to control the storage of the A/D data with an external signal in order to optimize the use of the on-board memory.

Gate Amplitude: TTL Level

Polarity: Active HIGH (store when HIGH, ignore when LOW)

Min. Pulse Width: 8 clock cycles

Rise/Fall Times: Must be faster than 10 ns

Connector: BNC on auxiliary PCB

## COOLING SYSTEM

Power Down: Software Controlled

Cooling Fan: Mounted on the A/D chip

## MULTI-CARD SYSTEMS

Operating Mode: Master/Slave or Multiple/Independent

Max. No. of Cards:

Master/Slave: 8

Multiple/Independent: Limited by backplane

## PCI BUS INTERFACE

Plug-&-Play: Fully supported

Bus Mastering: Fully supported

Bus Width: 32 bit

Bus Throughput: 100 MB/s to PC Memory

Compatibility: All PCI compliant computers

## INTERRUPTS

Interrupt Lines: 1 Line as per PCI specs PCI BIOS chooses the line

Interrupt on: Trigger, End of Capture, Memory Full, and others

## APPLICATION SOFTWARE

GageScope for DOS

## SOFTWARE SUPPORT

Software Development Kit for DOS
Available in source code in:
Borland C, Watcom C

Software Development Kit for Windows 95/98
Includes Sample Programs in Visual C++

Software Development Kit for Windows NT
Includes Sample Programs in Visual C++

MATLAB Software Development Kit
For Windows 95/98

MATLAB Software Development Kit
For Windows NT

LabVIEW Software Development Kit
For Windows 95/98

LabVIEW Software Development Kit
For Windows NT

## MATERIALS SUPPLIED

One CompuScope 8500 card
One CP500 Win 95/98 Driver Disk
(includes Quick Start Guide)
One CP500 Win NT Driver Disk
(includes Quick Start Guide)
One GageScope for DOS software package
(includes User Manual)
One Hardware Manual
One Disk Drive Power Cable

## WARRANTY

One year parts and labor

*All specifications subject to change without notice*

UPDATED 99/07/13

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Outside North America Tel. +514-633-7447 • Fax +514-633-0770 • E-mail: prodinfo@gage-applied.com • Web. www.gage-applied.com

# CompuGen 1100

## IBM PC Based High-speed Arbitrary Waveform Generator Card

CompuGen 1100 is a family of IBM PC based digital arbitrary waveform generator cards capable of providing aperiodic analog waveforms simultaneously with an independent TTL digital pattern generator.

### COMPUGEN 1100

Traditional waveform generators provide simple, periodic waveforms appropriate for audio and RF applications. The complex analog and digital circuits of today require the stimuli to be customized.

CG1100 enables the user to create a large number of varying analog and digital outputs and store them for future reference.

### CREATE AND EDIT WAVEFORMS

Arbitrary waveforms are generated by creating a digital representation of the waveform in the memory on-board CompuGen 1100. This digital pattern is then converted into an analog signal using a high speed DAC and amplifiers. The output gain and filtering can be set by software.

Arbitrary waveforms can be specified in several ways:

- Using equations
- Selecting from previously stored waveforms on disk
- Selecting from a library of standard waveforms
- Transferring data from CompuScope cards for replaying

### MEMORY DEPTH

One of the most powerful features of CompuGen 1100 is the huge on-board memory buffer it has.

With up to 16 Megasamples of on-board memory, CompuGen 1100 is one of the most powerful D/A cards in the world.

### CRYSTAL-BASED STABILITY

The CompuGen 1100 waveform synthesis is controlled by a stable 80 MHz crystal oscillator. This provides temperature stability, long-term stability and precision far above those available in standard waveform generators.

### MEMORY LOOPING

Memory looping allows the memory on-board CompuGen 1100 to be optimized.

For example, a 1000 point pattern can be repeated 100 times, thereby using up only 1000 words of on-board memory, instead of taking up 100,000 words of memory.

This feature makes CompuGen 1100 the most powerful arbitrary waveform generator on the market.

### ON-BOARD FILTER

CompuGen 1100 has an on-board selectable low pass filter for smoothing the output waveform by reducing the quantization error caused by the Digital to Analog Converter.

This software-controlled filter may be switched off when fast rising signals have to be generated.

### FAST AMPLIFIER

The amplifier used on the CompuGen 1100 has a very high output slew rate, 50Ω output impedance and output short protection up to ±50 Volts

### UP TO 80 MILLION CONVERSIONS PER SECOND

The CompuGen 1100 generates analog output at a maximum D/A conversion rate of 80 million samples per second (MS/s) with 12 bit vertical resolution.

### AMPLITUDE

The CompuGen provides a maximum output of ±10 Volts into a 1 kΩ load and a ±5 Volt output into a 50Ω load.

### 12 BIT RESOLUTION

The CompuGen 1100 provides 12 bit vertical resolution (4096 levels) on the output signal.

### TRIGGERING

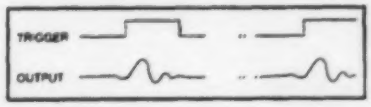
Internal and external trigger capability is provided for burst mode operation. An arbitrary waveform will be produced as a single burst on receiving a trigger either through software or by comparing the external trigger input with the level and slope set through software.

The trigger can also initiate periodic signal bursts timed through software

### RETRIGGERABLE MODE

Another triggering mode available on the CompuGen 1100 outputs the programmed signal every time a trigger occurs.

Once the generation of the output signal has ended, the trigger is re-armed in hardware. No software interaction is required




## COMPUGEN 1100 FEATURES

- **Up to 16 Megasamples of On-board Memory**
- **12 Bit Resolution**
- **80 Million Conversions per Second**
- **Free CGWin Software for Creating and Editing Waveforms**
- **Software Development Kits for DOS, Win 95/98/NT MATLAB and LabVIEW**

GaGe

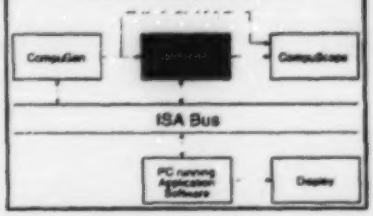
## INTEGRATION WITH COMPUSCOPE CARDS

CompuGen cards operate under software that can load and store GageScope files, i.e. files of data captured by CompuScope cards.

As such, the first level of integration between the two cards can be achieved using signal files. It is possible to capture a signal using a CompuScope and then recreate it with a CompuGen 1100.

Yet another level of integration can be achieved by using the two cards in the same system, with the application software controlling both cards using software drivers.

**Typical Test using a CompuGen and a CompuScope**




## PROGRAMMABILITY

The CompuGen 1100 is fully programmable for OEM applications. Software Development Kits are available for Windows 95, Windows 98 and Windows NT.

DOS-based SDKs with source code are available for Borland C, Visual C, and Watcom C.

Support is also available for MATLAB and LabVIEW.

## MULTI-CARD SYSTEMS

A Multi-Card system, comprising one Master and up to 7 Slave boards, can be ordered if more than one output channel is needed.

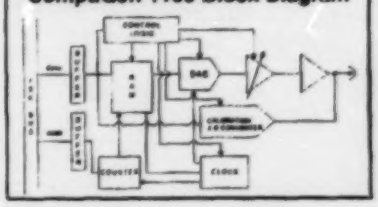
All signals necessary for synchronization of multiple CompuGen boards are passed from the Master to the Slave boards using a Master/Slave Interconnect.

These signals include the Conversion Clock, Trigger and other initialization signals.

## THREE-PHASE SIMULATION

Multiple CompuGen 1100 cards can be used to simulate three-phase voltage and current waveforms with control over the phase of each output

**CompuGen 1100 Block Diagram**



# COMPUGEN 1100 SPECIFICATIONS

## SYSTEM REQUIREMENTS

IBM PC AT or ISA bus compatible PC; 4MB RAM; 2 MB free space on hard drive; VGA Graphics card and monitor.

## SIZE

Single-slot full-length IBM PC/XT

## POWER (MAX)

| | |
|---|---|
| +5V | 15 W |
| +12V | 9 W |
| -12V | 1 W |
| -5V | 0.5 W |

## FEATURES

| | |
|---|---|
| Pattern Output: | Single Shot |
| Record Length: | 4 points min |
| Record Resolution: | 2 points |
| Trigger Modes: | Single, timed, or retriggerable |

## DIGITAL TO ANALOG CONVERSION

| | |
|---|---|
| Output: | 1 per card |
| Amplitude: | 20 Vp-p into 1 kΩ<br>10 Vp-p into 50 Ω |
| Resolution: | 12 bits |
| Accuracy: | ±2% excluding offset |
| Clock Frequency: | Max 80 MHz<br>Min 1 Hz |
| Conversion Rates: | 80 MHz, 40 MHz, 20 MHz |
| Output Frequency: | 10 MHz to 61 uHz |
| Buffer Depth: | 512K, 1M, 2M, 4M, 8M, or 16M samples |
| Full-scale Output Range: | ±100mV, ±200mV, ±500mV, ±1V, ±2V, ±5V<br>Voltages are specified with 50Ω termination. With no termination, voltage is doubled |
| Output Impedance: | 50Ω |
| Filter: | Software selectable (5 MHz, 10 MHz, 20 MHz, Infinite) |
| Output Protection: | Short-protected up to ±50V |
| Connector: | BNC |

## FREQUENCY STABILITY

| | |
|---|---|
| Long Term: | 100 ppm |

## TRIGGER

| | |
|---|---|
| Source: | Internal or External |
| External Trigger: | 0 to 5V TTL |
| Trigger Slope: | Rising or Falling |
| Connector: | BNC |

## EXTERNAL CLOCK (OPTIONAL)

| | |
|---|---|
| Clock Frequency: | Min DC, Max 80 MHz |
| Voltage: | 0 to 5V TTL |
| Connector: | BNC |
| Selection | Software selectable |

## MULTI-CARD SYSTEMS

| | |
|---|---|
| Max No of Cards: | 8 (1 master and 7 slaves) |
| Operating Mode: | Master/Slave or Multiple/Independent |

## APPLICATION SOFTWARE

CGWin Software (for Win 95/98/NT)

## SOFTWARE DEVELOPMENT KITS

Software Development Kit for DOS
Available in source code in:
Borland C, Watcom C

Software Development Kit for Win 95/98/NT
Includes Sample Programs in Visual C++

Software Development Kit for MATLAB
For Windows 95/98/NT

Software Development Kit for LabVIEW
For Windows 95/98/NT

## MATERIALS SUPPLIED

One CompuGen 1100 card
One CGWin Software for Windows (includes Win 95/98 and Win NT Drivers)
One Hardware Manual

## RECOMMENDED ACCESSORIES

50Ω Shunt

## WARRANTY

One year parts and labor

*All specifications subject to change without notice*

## ORDERING INFORMATION

### Hardware & Upgrades

| | |
|---|---|
| CompuGen 1100 - 512K | 110-101-001 |
| CompuGen 1100 - 1M | 110-101-002 |
| CompuGen 1100 - 2M | 110-101-003 |
| CompuGen 1100 - 4M | 110-101-004 |
| CompuGen 1100 - 8M | 110-101-005 |
| CompuGen 1100 - 16M | 110-101-006 |
| 512K to 1M Upgrade | 110-181-001 |
| 512K to 2M Upgrade | 110-181-002 |
| 512K to 4M Upgrade | 110-181-003 |
| 512K to 8M Upgrade | 110-181-004 |
| 512K to 16M Upgrade | 110-181-015 |
| 1M to 2M Upgrade | 110-181-005 |
| 1M to 4M Upgrade | 110-181-006 |
| 1M to 8M Upgrade | 110-181-007 |
| 1M to 16M Upgrade | 110-181-016 |
| 2M to 4M Upgrade | 110-181-008 |
| 2M to 8M Upgrade | 110-181-009 |
| 2M to 16M Upgrade | 110-181-017 |
| 4M to 8M Upgrade | 110-181-010 |
| 4M to 16M Upgrade | 110-181-018 |
| 8M to 16M Upgrade | 110-181-019 |
| External Clock Upgrade | 110-181-011 |
| Master Multi-Card Upgrade | 110-181-012 |
| Slave Multi-Card Upgrade | 110-181-013 |
| Periodic Re-Calibration | 110-181-014 |
| 50 Ohm Shunt | 110-111-001 |

### Software Development Kits (SDKs)

| | |
|---|---|
| Gage SDK Pack on CD | 200-113-000 |
| CompuGen SDK for Win 95/98/NT | 333-200-101 |
| CompuGen SDK for DOS | 333-200-100 |
| CompuGen SDK for MATLAB | 333-200-102 |
| CompuGen SDK for LabVIEW | 333-200-103 |

*All Upgrades performed at the factory*

**GAGE APPLIED SCIENCES INC.** 1233 Shelburne Rd., Suite 400, South Burlington, VT 05403 • Tel: 800-567-GAGE • Fax 800-780-8411
Outside North America Tel +514-633-7447 • Fax +514-633-0770 • E-mail prodinfo@gage-applied.com • Web www.gage-applied.com

## Appendix C- Celerity 750MS/s ADC and DAC specification sheets

# VME-ADC750

## 750 MHz Data Acquisition and Demultiplexer Card

### KEY FEATURES

- **High performance data acquisition and demultiplexing card**
- **6U-160 VME card with high speed FPDP and P2 output ports**
- **High speed analog and digital inputs**
- **750 MB/s maximum analog sample rate**
- **8 bit A/D converter**
- **40 dB spurious free dynamic range**
- **500 MHz input bandwidth**
- **64 Kbyte on-board FIFO**
- **100 MB/s digital interface (options to 750 MHz)**
- **FPDP style multiplexed data outputs directly compatible with Access256 systems for up to 6 GBytes of storage**
- **Easy to use control software and interface libraries**
- **Sun, PC, Mac, ALPHA, and embedded controller compatible**
- **Front end for GigaFLASH750 systems with up to 6 GBytes of high speed storage**
- **Master/slave control interface for fully coherent dual channel operation using two VME-ADC750s**

The CSI VME-ADC750 ultra high speed data acquisition/demultiplexer card provides unparalleled capability for digitizing wideband signals. With up to 750 MHz sampling rates at 8 bits, the VME-ADC750 card can digitize input signal data at bandwidths of 300 MHz. The card has up to 64 KBytes of high speed FIFO memory storage with direct outputs to the VMEbus interface or through a direct digital SnAP™ interface. It also serves as the front end to the GigaFLASH750™ wideband acquisition and storage systems with up to 6 gigabytes of total system high speed storage. These systems make use of the VME-ADC750's demultiplexed digital data FPDP ports, which are directly compatible with the digital input ports of the Access256™ data acquisition and storage modules. Together with the VME-DAC750 data playback/multiplexer cards, these modules provide integrated solutions for real world signal acquisition, storage, and high speed data transfer in a standard 6U VME form factor. The VME-ADC750 is the high end performer of the ultra high speed family of data acquisition cards, which includes the VME-ADC250 and the VME-ADC500 cards.

An analog input provides 8 bit digitization with 40 dB of spur-free dynamic range (typical). A digital data input allows parallel digital data recording at up to 100 MB/s rates. A unique feature of the system is the sneak-a-peek (SnAP) digital output which allows up to 64 Kbytes of data to be captured and passed to digital processors without interrupting the data being passed to the FPDP ports and recorded in the Access256 large memory buffers.

The VME-ADC750 can be controlled using Sun Sparcstation™, PC-compatible, Apple Macintosh™, and DEC ALPHA™ computers, as well as embedded 68040, '486, and Sparc VME processors. Software libraries, example programs, and analysis applications are available that simplify the process from initial hardware integration to operational results.

Applications include communications analysis, radar analysis, telecommunications processing and analysis, high speed analog-to-digital converter characterization, digital spectrum analysis, and high speed data buffering.

ULTRA WIDEBAND DATA ACQUISITION

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Celerity Systems Incorporated • 10411 Bubb Road • Cupertino, California 95014 • (408) 873-1001 • (408) 873-1397 FAX • http://www.csidaq.com

# VME-DAC750 High Speed Data Playback/Multiplexer Card

## System Overview

The CSI VME-DAC750 ultra high speed data playback/multiplexer card provides wide bandwidth digital signal reconstruction and arbitrary waveform generation from stored digital data. With up to 750 MHz sample rates at 8 bits, the VME-DAC750 card can reconstruct digital input signal data with bandwidths of up to 300 MHz. The card has up to 16 KBytes of high speed FIFO memory storage with direct inputs from the VMEbus interface. It also serves as the back end playback module to the GigaFLASH750™ wideband acquisition and storage systems with up to 6 Gigabytes of total system high speed storage. These systems make use of the VME-DAC750's six multiplexed digital data "MDD" ports, which are directly compatible with the digital output ports of the Access256™ data storage and playback modules. Together with the VME-ADC750 data acquisition/demultiplexer cards, these modules provide integrated solutions for real world signal acquisition, storage, playback, and high speed data transfer in a standard 6U VME form factor. The VME-DAC750 is the high end performer of the ultra high speed family of data playback and reconstruction cards, which includes the VME-DAC250 and the VME-DAC500 cards.

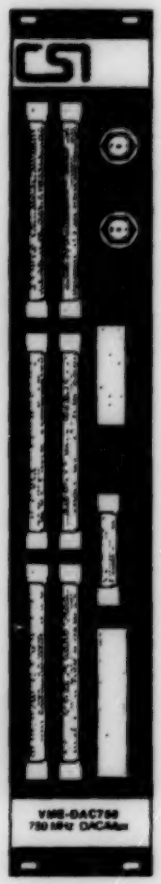
An analog output provides 8 bit digitization with 40 dB of spur-free dynamic range at up to 100 MB/s (with options to 750 MB/s). A digital data output allows parallel digital data playback at up to 100 MB/s rates, with options to 750 MB/s rates. A motherboard/ daughtercard architecture separates the multiplexed digital data "MDD" ports, FIFO storage, multiplexing, and VME controls from the high speed digital fan in and analog DAC reconstruction.

The VME-DAC750 can be controlled using Sun Sparcstation™, PC-compatible, Apple Macintosh™, and DEC ALPHA™ computers, as well as embedded 68040, '486, and Sparc VME processors. Software libraries, example programs, and applications are available that simplify the process from initial hardware integration to operational results.

Applications include communications signal synthesis, radar waveform generation, telecommunications processing and analysis, high speed digital-to-analog converter characterization, and digital arbitrary waveform generation.

## System Features

- High performance digital data reconstruction and multiplexing
- High speed analog and digital outputs
- 750 MS/s maximum analog sample output rate (with option 1, 100 MS/s is standard)
- 8 bit D/A converter
- 500 MHz output bandwidth (with option 1)
- 100 MB/s maximum digital output rate (750 MB/s with option 2)
- VME control and data transfer
- Easy-to-use control software and interface libraries
- Sun, PC, Mac, ALPHA, and embedded controllable
- Six high speed multiplexed digital data "MDD" ports directly compatible with Access256 systems
- Back end for GigaFLASH750 systems with up to 6 GBytes of high speed storage



VME-DAC750 Data Playback Card

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## Appendix D- Gray Chip digital receiver GC4114

# GC4114 DATASHEET

## 1.0 KEY FEATURES

- Four identical up-convert channels
- Independent modulation frequencies
- Independent phase/gain controls
- The four input signals are summed into a single output signal
- Maximum output rate of 62.5 MHz
- 16 bit real or complex inputs
- Interpolation factors of
  16 to 32,768 in the real input mode
  32 to 65,536 in the complex input mode
- Bit serial input format, or
- Memory mapped input registers
- 8 to 16 bit output samples
- 2's Complement or offset-binary output format
- 0.02 Hz tuning resolution
- 90 dB Spur Free Dynamic Range
- > 90 dB far image rejection
- > 70dB near image rejection
- 0.07 dB gain resolution
- 0.05 dB peak to peak passband ripple
- User programmable 63 tap input filter
- Accepts QPSK or QAM symbol data directly, performs transmit (pulse shape) filtering
- Meets Damps and GSM specifications
- Sum I/O path to merge outputs from multiple GC4114 chips
- Microprocessor interface for control, input, and diagnostics
- Built in diagnostics
- Microprocessor and serial inputs will accept either 3.3 or 5 volt input levels.
- 800 mW at 33 MHz, 3.3 volts
- 100 pin thin QFP package

## 2.0 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1.

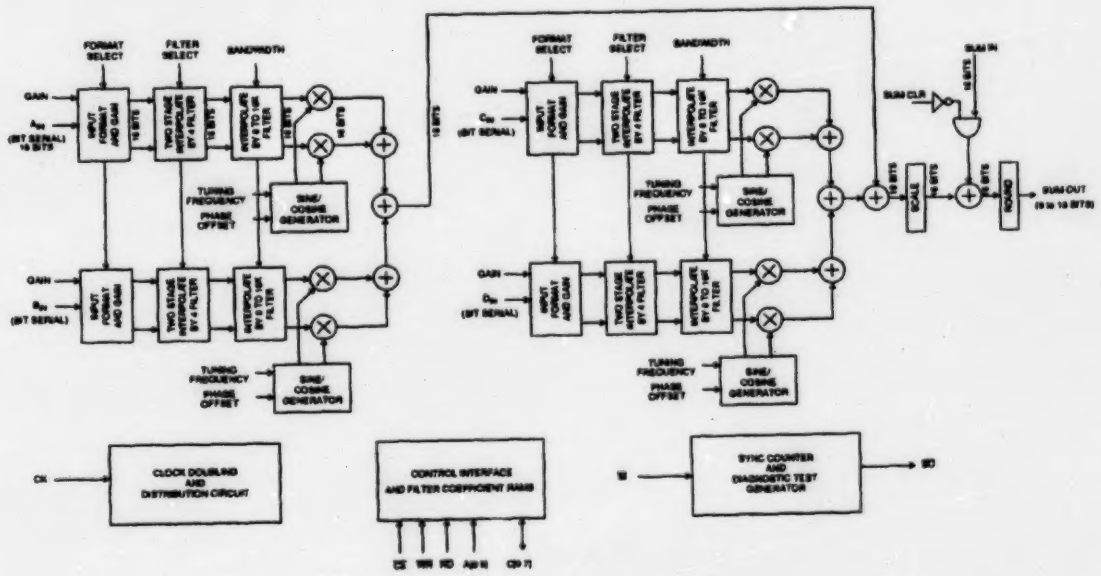


Figure 1. GC4114 Block Diagram



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## 3.0 FUNCTIONAL DESCRIPTION

The GC4114 quad transmit chip contains four identical up-conversion circuits. Each up-convert circuit accepts a real or complex signal, interpolates it by a programmable factor ranging from 32 to 65,536 (16 to 32,768 for single-sideband modulation), up-converts the signal to a selected center frequency, sums it with other up-converted samples and outputs the combined signal. The chip contains a user programmable input filter which can be used to shape the transmitted data, or can be used as a Nyquist transmit filter for digital data transmission. See the application notes in Section 7.5 for details on using the chip to transmit QPSK or QAM data.

The up-converters are designed to maintain over 90 dB of spur free dynamic range and image rejection. Each up-convert circuit accepts 16 bit inputs (bit serial) and produces 16 bit outputs. The up-converter outputs are summed with an external 16 bit input to produce a single 16 bit output. The frequencies and phase offsets of the four sine/cosine sequence generators can be independently specified, as can the gain of each circuit. The up-converters share the same bandwidth, filter coefficients and input formats.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of an 8 bit data I/O port, a 6 bit address port, a chip enable strobe, a read strobe and a write strobe. The chip's 64 control registers (8 bits each) are memory mapped into the 6 bit address space of the control port.

### 3.1 CONTROL INTERFACE

The chip is configured by writing control information into sixty four control registers within the chip. The contents of these control registers and how to use them are described in Section 5. The registers are written to or read from using the **C[0:7]**, **A[0:5]**, $\overline{\text{CE}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins. Each control register has been assigned a unique address within the chip. This interface is designed to allow the GC4114 to appear to an external processor as a memory mapped peripheral (the pin $\overline{\text{RD}}$ is equivalent to a memory chip's $\overline{\text{OE}}$ pin).

An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:5]** to the desired register address, selecting the chip using the $\overline{\text{CE}}$ pin, setting **C[0:7]** to the desired value and then pulsing $\overline{\text{WR}}$ low. The data will be latched on the rising edge of $\overline{\text{WR}}$ or $\overline{\text{CE}}$.

To read from a control register the processor must set **A[0:5]** to the desired address, select the chip with the $\overline{\text{CE}}$ pin, and then set $\overline{\text{RD}}$ low. The chip will then drive **C[0:7]** with the contents of the selected register. After the processor has read the value from **C[0:7]** it should set $\overline{\text{RD}}$ and $\overline{\text{CE}}$ high. The **C[0:7]** pins are turned off (high impedance) whenever $\overline{\text{CE}}$ or $\overline{\text{RD}}$ are high or when $\overline{\text{WR}}$ is low. The chip will only drive these pins when both $\overline{\text{CE}}$ and $\overline{\text{RD}}$ are low and $\overline{\text{WR}}$ is high.

One can also ground the $\overline{\text{RD}}$ pin and use the $\overline{\text{WR}}$ pin as a read/write direction control and use the $\overline{\text{CE}}$ pin as a control I/O strobe.


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## Appendix E- Motorola Altivec processor(G4) specification overview

**Fact Sheet**

# AltiVec™ Technology

## Motorola's High-Performance Vector Parallel Processing Expansion to the PowerPC Architecture™

Motorola's new AltiVec technology expands the capabilities of PowerPC™ microprocessors by providing leading-edge, general-purpose processing performance while concurrently addressing high-bandwidth data processing and algorithmic-intensive computations in a single-chip solution.

Traditionally, many high-performance applications have contained a combi of a single microprocessor performing the system control function and off- devices based on one or more other architectures, such as a DSP farm or ci tom ASICs, to perform specialized computations. AltiVec technology will enable a new class of processors that provides for the convergence of these technologies. AltiVec technology provides embedded and computing system designers with a new "one part—one code base" approach to product design. Because this integrated solution is still 100% compatible with the industry standard PowerPC architecture, design and support are simplified and the development barriers inherent to multiple architecture designs are eliminated. System designers and their customers will benefit through the reduced time-to-market and lowered total system development expense while simultaneously enjoying a tremendous jump in performance.

## New Execution Unit & New Instructions Provide New Capabilities

Motorola's AltiVec technology expands the current PowerPC architecture through the addition of a 128-bit vector execution unit, which operates concurrently with the existing integer and floating point units. This new engine provides for highly parallel operations, allowing for the simultaneous execution of up to 16 operations in a single clock cycle.

AltiVec technology is a short vector parallel architecture. Depending on data size, vectors are 4, 8 or 16 elements long. This can be contrasted with the long vector architectures of supercomputers that were popular in the 1980s. Vector sizes for those machines ranged to hundreds of elements. The long vector approach of supercomputers, while useful for scientific calculations, is not optimal for the communications, multimedia and other performance-driven applications targeted by Motorola with AltiVec technology.

AltiVec technology operations are performed on multiple data elements by a single instruction. This is often referred to as SIMD (single instructions, multiple data) parallel processing. AltiVec technology offers support for:

- 16-way parallelism for 8-bit signed and unsigned integers and characters
- 8-way parallelism for 16-bit signed and unsigned integers
- 4-way parallelism for 32-bit signed and unsigned integers and IEEE floating-point numbers

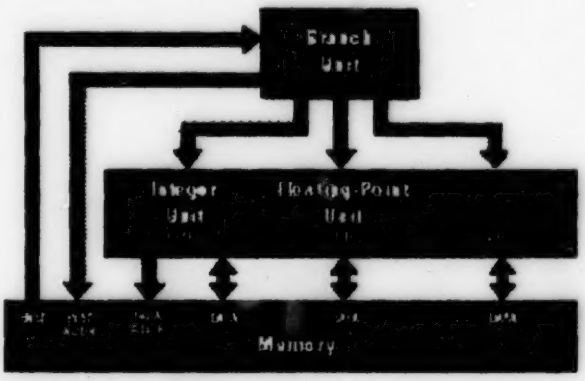
AltiVec technology also includes a separate register file containing 32-entries, each 128-bits wide. These 128-bit wide registers hold the data sources for the AltiVec technology execution units. Registers are loaded and unloaded through vector store and vector load instructions that transfer the contents of a single 128-bit register to and from memory.

PowerPC™

MOTOROLA

AltiVec technology can be most accurately thought of as a set of registers and execution units added to the PowerPC architecture in an analogous manner to the addition of floating point units. Floating point units were added to most mainstream microprocessor architectures to provide better support for high-precision scientific calculations. AltiVec technology is being added to the PowerPC architecture to dramatically accelerate the next level of performance-driven, high-bandwidth communications and computing applications.

**High-level structural overview for PowerPC with AltiVec technology**




Each AltiVec instruction specifies up to three source operands and a single destination operand. All operands are vector registers, with the exception of the load and store instructions and a few instruction types that provide operands from immediate fields within the instruction. 162 new unique instructions are defined for the AltiVec technology. These instructions fall into the following major classes:

- Intra-element arithmetic operations
- Inter-element arithmetic operations
- Intra-element non-arithmetic operations
- Inter-element non-arithmetic operations

## Applications of AltiVec Technology

The initial target applications for PowerPC processors utilizing AltiVec technology include:

- IP telephony gateways
- Speech processing systems
- Image and video processing systems
- Internet routers
- Multi-channel modems,
- Echo cancelers
- Scientific array processing systems
- Virtual private network servers.

In addition to accelerating next-generation applications, AltiVec technology can, through its wide datapaths and wide field operations, also accelerate many time-consuming traditional computing and embedded processing operations such as memory copies, string compares and page clears.

Unlike fixed function solutions which are most often implemented as application specific integrated circuits, AltiVec technology will offer a programmable solution that can easily migrate via software upgrades to follow changing standards and customer requirements. The preferred programming environment is the C and C++ languages favored by embedded systems developers. Motorola is working with leading tools providers to develop simulators, assemblers, linkers and compilers to assure full support for the AltiVec technology.

While the initial PowerPC microprocessor utilizing AltiVec technology will target very high-performance applications in networking and computing applications, subsequent Motorola processors with AltiVec technology could address markets and applications in which performance must be balanced with power, price and peripheral integration.

## Contact Information

- For more information on AltiVec technology, including programming models and white papers, visit Motorola's AltiVec Technology website at:

  **http://motorola.com/AltiVec/**

- For additional information:
  Call: 800-845-6686, or your local Motorola sales representative.

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## Appendix F- Calculation for Estimated Performance of Demonstration System

Using the components recommended in section 3.3., the time line in Figure 2, and assumptions from section 3.4, the analysis of performance can be estimated for different radars. In [3] the estimation of processing power in floating point operations per second per tap (range target) is given as

$$Y_o = 10\,\tau\,\beta\,PRF \tag{4}$$

Where:
- $\tau$ is the pulse width
- $\beta$ is the radar bandwidth for the pulse
- PRF is the radar pulse repetition frequency

For our analysis we wish to change two things about this equation. First, the constant 10 should be increased to account for an increase in assumed sampling rate margin above Nyquist criteria from 25% to 50%. Secondly, equation (4) assumes that the entire PRI is available for calculation time, yet the time line introduced in Figure 2 suggests that for this hardware implementation there is far less that the entire PRI available. We replace the PRF variable with $(1/t_{CALC})$, the inverse of the time available for calculation. The new equation becomes

$$Y_o = 1.5*8\,\tau\,\beta\,(1/t_{CALC})$$

$$= 12\,\tau\,\beta\,/t_{CALC} \tag{5}$$

The time available for calculations ($t_{CALC}$) is the PRI less the pulse width ($\tau$), less the time for data transfer ($t_{TRF}$) in and out of working memory:

$$t_{CALC} = PRI - \tau - 2 * t_{TRF}. \tag{6}$$

The time for data transfer is the $Memory_{per\ pulse}$, given in equation (3) in section 2.2, divided by the transfer rate. For our purposes the sampling frequency ($F_s$) is 1.5 times the radar bandwidth, and the memory per sample ($M_s$) is 2 bytes, one each for inphase and quadrature.
Note that equation (3) is: $Memory_{per\ pulse} = F_s\,\tau\,M_s$.

$$t_{TRF} = (1.5\,\beta\,\tau\,2) / (90\% * 45\ MB/s) \tag{7}$$

The number of range targets ($n_{RT}$) that can be produced is the number of effective operations per second divided by the number of required operations per second per range target.

$$n_{RT} = EOPS / Y_o \quad (8)$$

Equation 8 can be solved by successively substituting equations 5,6 and 7 into equation 8, and then using values of $\tau$, $\beta$ and PRI corresponding to the radar in question.

Alternative time line assumptions could be used if time constraints are too tight or further performance is sought. Other time lines may include multiple PRI delays to obtain the computed result, using the same captured pulse for computation of several calculated returned pulses, or using a fraction of the full pulse for computation. Some of these listed alternatives may degrade the quality of CECM, and would require further study before being adopted.

## List of Symbols, Abbreviations, Acronyms and Initialisms

| | |
|---|---|
| β | Radar Bandwidth |
| μs | Microsecond |
| τ | Pulse Width |
| ADC | Analog to Digital Converter |
| AGC | Automatic Gain Control |
| BW | Bandwidth |
| CCRS Convair-580 | Canadian Center for Remote Sensing Convair 580 Airborne SAR System |
| CECM | Computed Electronic Countermeasure |
| COTS | Commercial-Off-The-Shelf |
| cPCI | Compact PCI |
| DAC | Digital to Analog Converter |
| dB | Decibel |
| DSP | Digital Signal Processor |
| ENOB | Effective Number Of Bits |
| EOPS | Effective Operations Per Second |
| E-SAR, ERS, SIR-C | SAR imaging radars |
| FFT | Fast Fourier Transform |
| FIR | Finite Impulse Response |
| GS/s | GigaSamples per Second |
| HPRF | High Pulse Repetition Frequency |
| Hz | Hertz |
| I/Q | In-phase and Quadrature |
| MB/s | Megabytes per Second |
| MHz | MegaHertz |
| MPRF | Medium Pulse Repetition Frequency |
| MS/s | MegaSamples per Second |
| PCI | Peripheral Component Interconnect bus |
| PHARUS | Polarimetric PHased ARray Universal SAR |
| PRF | Pulse Repetition Frequency |
| PRI | Pulse Repetition Interval |
| PW | Pulse Width |
| RADARSAT | A Canadian RADAR SATellite |
| SAR | Synthetic Aperture Radar |
| SQNR | Signal-to-Quantization-Noise Ratio |
| TG | Techniques Generator |
| TOA | Time Of Arrival |
| TTT | Time To Transmit |
| VME | VersaModule Eurocard bus |
| X-SAR | X band Synthetic Aperture Radar |

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Computed Electronic Countermeasures System Implementation Investigation (U)

4. AUTHORS (Last name, first name, middle initial)

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| 5 DATE OF PUBLICATION (month and year of publication of document) | 6a. NO OF PAGES (total containing information Include Annexes, Appendices, etc ) | 6b. NO OF REFS (total cited in document) |
|---|---|---|
| Aug 2000 | 54 | 14 |

7. DESCRIPTIVE NOTES (the category of the document, e g technical report, technical note or memorandum. If appropriate, enter the type of report, e g interim, progress, summary, annual or final Give the inclusive dates when a specific reporting period is covered.)

Contractor Report

8. SPONSORING ACTIVITY (the name of the department project office or laboratory sponsoring the research and development Include the address.)

Defence Research Establishment Ottawa
National Defence
Ottawa, Ontario K1A 0Z4

| 9a. PROJECT OR GRANT NO (If appropriate, the applicable research and development project or grant number under which the document was written Please specify whether project or grant) | 9b. CONTRACT NO. (if appropriate, the applicable number under which the document was written) |
|---|---|
| 5BB25 | W7714-9-0259 |

| 10a. ORIGINATOR'S DOCUMENT NUMBER (the official document number by which the document is identified by the originating activity This number must be unique to this document ) | 10b OTHER DOCUMENT NOS (Any other numbers which may be assigned this document either by the originator or by the sponsor) |
|---|---|
| DREO CR 2000-066 | |

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This report presents and discusses the issues involved in implementing computer electronic countermeasures (CECM) within a jammer system. Further, the report presents an initial proof of concept demonstration system, its upgrade path and estimated performance. Computed electronic countermeasures are countermeasures where the transmitted signal is digitally formed entirely or in large part using one or more programmable digital computers. By using a digital representation of a radar pulse, the signal can be mathematically modified by computation in software to model the echo signals for arbitrary false targets.

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